A Study of Interference in Synchronous Systems

Tsutomu Yoshimura, *Member, IEEE*, and Atsushi Iwata, *Member, IEEE*

***Abstract*—The influence of interference and coupling in synchronous systems is investigated. Our new approach based on the linear time-variant model in oscillatory systems lends new insight into interference and coupling phenomena in synchronous systems. According to the analysis, it is possible that a small perturbation to an oscillator is enhanced by positive feedback through coupling with another oscillatory system. This implies that the inherent phase error caused by thermal noise can lead to a large amount of jitter by interference even in the absence of external noise. The analysis also reveals the relationship between the jitter occurrence and frequency difference in a plesiochronous system. Additionally, it is shown that the coupling within a closed-loop system can limit the bandwidth of a phase-locked loop and cause the peak gain of the response of the phase error. We confirmed these analytical results by measurements conducted on test chips.**

***Index Terms*—Interference, phase-locked loops (PLLs), jitter, phase noise, stability, feedback, substrate noise, power supply noise, synchronization, mesochronous.**

I. Introduction

THE continued scaling of CMOS process technologies has facilitated the integration of high-speed interface circuits, large-scale digital cores, and analog circuits on a chip. The issue of interference noise becomes increasingly important for realizing such system on devices. Many interference cases exist: the interference between a transmitter and receiver, analog circuits and digital cores, different clock domains, etc. In particular, the interference noise between clock domains hampers chip performance. Injection locking and injection pulling between two oscillators are examples of undesirable phenomena caused by interference noise [1]. Recently, a lot of investigations of the phase noise in oscillators have been reported [2]–[4], where the inherent device noise such as thermal noise is treated as the main noise source in oscillators. On the other hand, the studies of the phase noise or the timing jitter in oscillators subject to the supply noise and the substrate noise have been reported [5], [6]. In [5], the timing jitter in ring oscillators due to the supply and substrate noise was evaluated in terms of two kinds of figure of merits: the cycle jitter and the cycle-to-cycle jitter. Heydari investigated the properties of the power supply and the substrate noise and proposed a stochastic impulse train as the substrate noise model [6]. He employed this model for the calculation of the phase noise of the output of phase-locked loops (PLLs). In both [5] and [6], the noise injected into oscillators is defined as external and non-correlated to the output of the oscillators.

Manuscript received April 29, 2005; revised December 5, 2005, and March 7, 2006. This paper was recommended by Associate Editor G. Palumbo.

T. Yoshimura is with Mitsubishi Electric Corporation, Hyogo 664-8641, Japan (e-mail: Yoshimura.Tsutomu@eb. MitsubishiElectric.co.jp).

A. Iwata is with the Faculty of Engineering, Hiroshima University, Higashi-Hiroshima 739-8527, Japan (e-mail: iwa@dsl.hiroshima-u.ac.jp).

Digital Object Identifier 10.1109/TCSI.2006.879061

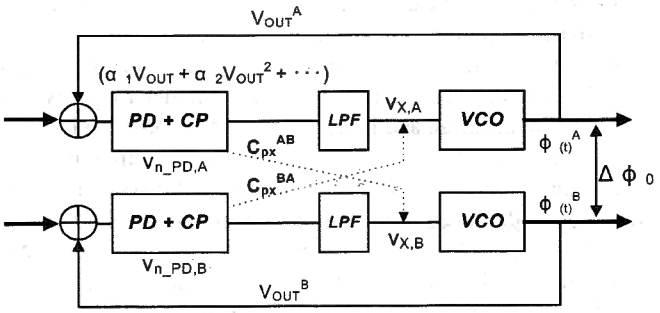


Fig. 1. Two closed loops with interference noise.

This study investigates the influence of the interference noise and coupling noise in synchronous systems. For analyzing the interference between two oscillatory systems, we consider two types of synchronous systems: a mesochronous system and a plesiochronous system [7]. In the mesochronous system, two oscillators operate synchronously at the same frequency; however, they are in an arbitrary phase with respect to each other. In the plesiochronous system, an oscillator operates at a frequency that is slightly different from that of the other oscillators, and a slow phase drift occurs. We also investigate the effect of the coupling noise in a closed-loop system with one oscillator.

In general, the abovementioned phenomena can be understood by analyzing the time-variant model [2]. Our new approach based on the linear time-variant (LTV) model will provide an insight for analyzing the influence of the interference noise between oscillatory systems and the coupling noise within a single clock domain.

Theoretical approaches for analyzing the influence of interference and coupling are illustrated in Section II, wherein we discuss the condition under which closed-loop systems may enter unstable states due to interference or coupling. In Section III, we describe the supply lines and the substrate model for the coupling simulation. Further, we demonstrate the technique that controls the coupling between adjacent closed-loop systems by simulation. Section IV shows the measurement results of mesochronous, plesiochronous, and synchronous systems. Section V concludes the paper.

II. Analysis of Interference in Closed-Loop Systems

A. Block Diagram of the Interference Model in Two Oscillatory Systems

Fig. 1 shows the block diagram of oscillatory systems with interference noise. It consists of two PLLs that are coupled with each other [8].

With regard to the interference between two closed loops, we make the following assumptions.

1057-7122/$20.00 © 2006 IEEE

- The oscillation frequencies of the two PLL are the same or very close to each other.
- The noise source is the charging current flow to the load in digital circuits such as phase detectors and charge pumps [9].
- The noise in one digital circuit causes a voltage fluctuation in the loop filter node of the other closed-loop system.
- The above mentioned noise and voltage fluctuation are related to each other through a fixed parameter C_{px}, which is time invariant and independent of the noise level.

The coupling of the power supply and the substrate noise to oscillators is generally defined as the stochastic noise model in the large-scale mixed analog-digital integrated circuits [6]. The statistical approaches are needed to characterize the jitter in that case. To adopt the stochastic model assumes that the supply and the substrate noise are noncorrelated or less correlated to the output signal. On the other hand, the interference noise between the above oscillatory systems is strongly correlated to the each output signal. Therefore, we have to show the relationship between the interference noise and the fluctuation of output signal to characterize the influence of interference in our model.

B. Analysis of Interference Noise in Mesochronous Systems

First, we investigate the influence of interference in mesochronous systems. In order to analyze the phase noise of oscillators with interference noise, the concept of the impulse sensitivity function (ISF) is applied to this system [2], [10], [11]. The sensitivity of a voltage-controlled oscillator (VCO) to the loop filter can be expressed as follows:

$$\Gamma \equiv \left.\frac{\delta\phi(t)}{v_X \delta t}\right|_{t=\tau} = \frac{C_0}{2} + \sum_k C_k \cos(k\omega_0\tau + \theta_k) \quad (1)$$

where ω_0 is the oscillation frequency; θ_k is the phase of the kth harmonic; and C_k is the coefficient of the Fourier series of the ISF. The variable v_X is the voltage displacement injected to the control node of the VCO. Note that this ISF is not dimensionless and is defined by the displacement of the voltage instead of the current.

The applicability of the ISF to the sensitivity of a VCO is verified by the following discussion.

As shown in [2, Fig. 6], it is required for the phase error of the oscillator to be proportional to the injection charge

$$\frac{\delta\phi(t)_{i\_\text{noise}}}{\Delta q} = \text{const}(\equiv \Gamma_{i\_\text{noise}}) \quad (2)$$

where $\delta\phi(t)_{i\_\text{noise}}$ is the phase error induced by the injection charge in [2] and Γ_{i_noise} is the impulse sensitivity function of the oscillator. On the other hand, it is obvious that the voltage displacement to the control node and the frequency variation of the VCO follow the relationship mentioned below

$$\frac{\delta\omega(t)}{v_X} = \frac{(\delta\phi(t)/\delta t)}{v_X} = \text{const}(\equiv \Gamma) \quad (3)$$

where $\delta\omega(t)$ is the frequency difference from ω_0 which is the oscillation frequency of the VCO without any voltage displacement to the control node. Since the oscillation frequency is proportional to the voltage of the control node of the VCO within the range of the first-order approximation, most of VCOs satisfy (3). The ISF is the periodic function of the oscillation frequency ω_0; therefore, it can be expanded as (1).

The sinusoidal noise to the loop filter, which is equivalent to the injection noise to the control node of the VCO, is assumed as

$$v_X \equiv v_{X0}\cos[(\omega_0 + \Delta\omega)t + \theta_{n0}] \quad (4)$$

where $\Delta\omega$ is the frequency offset from the carrier and θ_{n0} is the initial phase of the additional noise to the filter. The phase error of the VCO is obtained as follows:

$$\begin{aligned}\phi(t)_{\text{open}} &= \int^t v_X \cdot \Gamma \, d\tau \\ &\approx \frac{v_{X0}\cdot C_1}{2\Delta\omega}\sin(\Delta\omega t + \theta_{n0} - \theta_1). \end{aligned} \quad (5)$$

In the case of a closed loop, the phase error of the sideband of the carrier is suppressed. When $\Delta\omega$ is within the range $(\omega_n)/(2\zeta) < \Delta\omega < 2\zeta\omega_n(\equiv \omega_C)$ (where ω_n and ζ are the natural frequency and damping factor of the PLL, respectively), the phase error of the closed loop is attenuated by the feedback system and is derived as follows:

$$\phi(t)_{\text{close}} \equiv \phi(t) = \frac{v_{X0}\cdot C_1}{2\omega_C}\sin(\Delta\omega t + \theta_{n0} - \theta_1). \quad (6)$$

By setting the initial value of time so that $\theta_{n0} - \theta_1 = 0$, the clock waveform V_{out} can be expressed as

$$\begin{aligned} V_{\text{OUT}} &\prec \cos(\omega_0 t + \phi(t)) \\ &= \cos\left(\omega_0 t + \frac{v_{X0}\cdot C_1}{2\omega_C}\sin(\Delta\omega t)\right) \\ &\cong \cos(\omega_0 t) + \frac{v_{X0}\cdot C_1}{4\omega_C} \\ &\quad \times [\cos(\omega_0 + \Delta\omega)t - \cos(\omega_0 - \Delta\omega)t] \end{aligned} \quad (7)$$

where we use the following approximation [12]:

$$\begin{aligned} &\cos(\omega_0 t + m_p \sin(\Delta\omega t)) \\ &\quad \approx \cos(\omega_0 t) + \frac{m_p}{2}[\cos((\omega_0 + \Delta\omega)t) \\ &\qquad - \cos((\omega_0 - \Delta\omega)t)]. \end{aligned} \quad (8)$$

The noise of the digital block V_{n_dig} induced by the clock operation is considered to be a nonlinear function of the clock and is described as

$$v_{n\_\text{dig}} = \alpha_1 V_{\text{OUT}} + \alpha_2 V_{\text{OUT}}^2 + \cdots. \quad (9)$$

Since we consider a linear model, the noise element of the digital block is given by

$$v_{n\_PD,A} = \alpha_1 \frac{v_{X0}\cdot C_1}{4\omega_C}\cos(\omega_0 + \Delta\omega)t. \quad (10)$$

The above noise is added to the loop filter node of the other PLL by using the coupling parameter C_{px}

$$v_{X,B} = C_{px}^{AB} \cdot \alpha_1 \cdot \frac{v_{X0} \cdot C_1}{4\omega_C} \cos(\omega_0 + \Delta\omega)t \qquad (11)$$

where the parameter C_{px}^{AB} implies the coupling from PLL A to B. Since we assume that the two PLLs have the same properties, we usually omit the suffixes A or B in the other parameters.

By repeating the procedure, the clock waveform in the other PLL is given by

$$V_{\mathrm{OUT},B} \prec \cos\left[\omega_0 t + \phi(t)^B + \Delta\phi_0\right] = \cos\left[\omega_0 t + \frac{C_{px}^{AB} \cdot \alpha_1 \cdot v_{X0}}{8} \cdot \left(\frac{C_1}{\omega_C}\right)^2 \times \sin(\Delta\omega t - \theta_1) + \Delta\phi_0\right] \qquad (12)$$

where $\Delta\phi_0$ is the relative phase difference between two oscillatory systems. In the mesochronous system, this value is time invariant.

Using the coupling parameter C_{px}^{BA}, the noise from the other PLL to the loop filter is expressed as follows:

$$v_{X,A} = C_{px}^{BA} \cdot v_{n\_PD,B} = C_{px}^{BA} \cdot \alpha_1 \cdot \cos\left[\omega_0 t + \frac{C_{px}^{AB} \cdot \alpha_1 \cdot v_{X0}}{8}\left(\frac{C_1}{\omega_C}\right)^2 \times \sin(\Delta\omega t - \theta_1) + \Delta\phi_0\right]. \qquad (13)$$

If we assume that $\theta_1 = \theta_{n0} = 0$ and $\Delta\phi_0 = 0$, (13) is expanded as follows:

$$v_{X,A} \cong C_{px}^{BA} \cdot \alpha_1 \left[\cos\omega_0 t + \frac{C_{px}^{AB} \cdot \alpha_1 \cdot v_{X0}}{16} \cdot \left(\frac{C_1}{\omega_C}\right)^2 (\cos(\omega_0 + \Delta\omega)t - \cos(\omega_0 - \Delta\omega)t)\right]. \qquad (14)$$

The signals at a frequency of $\omega_0 + \Delta\omega$ are obtained from (4) and (14).

A) The input noise to the loop filter is given as follows:

$$v_{X(\mathrm{IN})} = v_{X0} \cos(\omega_0 + \Delta\omega)t. \qquad (15)$$

B) The output noise caused by coupling with another PLL

$$v_{X(\mathrm{OUT})} = \frac{C_{px}^{AB} \cdot C_{px}^{BA} \cdot \alpha_1^2 \cdot v_{X0}}{16} \cdot \left(\frac{C_1}{\omega_C}\right)^2 \cos(\omega_0 + \Delta\omega)t. \qquad (16)$$

When the peak value of the output noise exceeds the input noise, it is possible that a small perturbation to the loop filter will be enhanced by positive feedback. This implies that the inherent phase error caused by thermal noise may cause a significant jitter. In this analysis, we first consider a small perturbation noise to the filter; it shows that the interference between two oscillatory systems can result in a large phase error without any external noise, as summarized below.

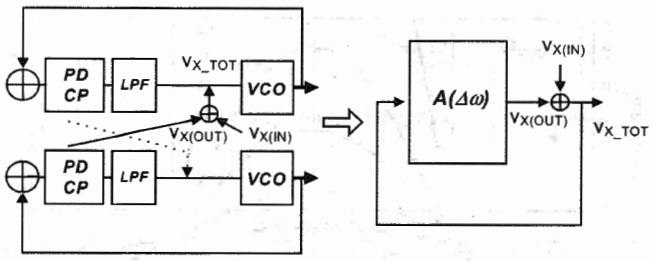


Fig. 2. Interference model of the two closed loops and the equivalent closed-loop model.

I) When $(C_{px}^{AB} \cdot C_{px}^{BA} \cdot \alpha_1^2)/(16) \cdot ((C_1)/(\omega_C))^2 \geqslant 1$, a large amount of jitter may result from the interference between two oscillatory systems.

II) When $(C_{px}^{AB} \cdot C_{px}^{BA} \cdot \alpha_1^2)/(16) \cdot ((C_1)/(\omega_C))^2 < 1$, a small perturbation to the loop filter is suppressed and it does not increase to a large jitter.

Here, we consider the phase margin of the abovementioned interference system. The interference model of the two oscillators may be considered to be a closed-loop one, as shown in Fig. 2.

The total noise V_{X_TOT} of the interference model shown in Fig. 2 is represented by using a closed-loop model as follows:

$$A(\Delta\omega) \cdot V_{X\_\mathrm{TOT}} + V_{X(\mathrm{IN})} = V_{X\_\mathrm{TOT}} \quad \therefore \frac{V_{X\_\mathrm{TOT}}}{V_{X(\mathrm{IN})}} = \frac{1}{1 - A(\Delta\omega)}. \qquad (17)$$

Therefore, when $A(\Delta\omega) = 1$, the response function becomes infinite and the system enters an unstable state. In other words, when $\angle A(\Delta\omega) = 0$ and $A(\Delta\omega) \geqslant 1$, the system has no phase margin and enters an unstable state [13].

Next, consider the general case: $\theta_1 = \theta_{n0} \neq 0$ and $\Delta\phi_0 \neq 0$. The input and output noises to the loop filter are described in (4) and (13), respectively. In order to determine the condition under which a small perturbation to the filter can be enhanced, a function is defined as follows (see Appendix I):

$$\begin{aligned} &\left\| v_{X(\mathrm{OUT})} \bullet \left(v_{X(\mathrm{IN})}/v_{X0}\right)\right\| \\ &\equiv \lim_{t\to\infty} \frac{\int^t v_{X(\mathrm{OUT})}(\tau) \cdot \left(v_{X(\mathrm{IN})}(\tau)/v_{X0}\right) d\tau}{\int^t \left(v_{X(\mathrm{IN})}(\tau)/v_{X0}\right)^2 d\tau} \\ &\cong \lim_{t\to\infty} \frac{1}{(1/2)\cdot t} \cdot \frac{C_{px}^{BA} \cdot \alpha_1}{2} \int^t d\tau \Bigg\{ \\ &\quad \times \cos\left[(2\omega_0 + \Delta\omega)\tau + \theta_1 + \Delta\phi_0 + \frac{C_{px}^{AB}\alpha_1 \cdot v_{X0}}{8} \cdot \left(\frac{C_1}{\omega_C}\right)^2 \sin(\Delta\omega\tau - \theta_1)\right] \\ &\quad + \cos\left[\Delta\omega\tau + \theta_1 - \Delta\phi_0 - \frac{C_{px}^{AB}\alpha_1 \cdot v_{X0}}{8} \cdot \left(\frac{C_1}{\omega_C}\right)^2 \sin(\Delta\omega\tau - \theta_1)\right]\Bigg\}. \end{aligned} \qquad (18)$$

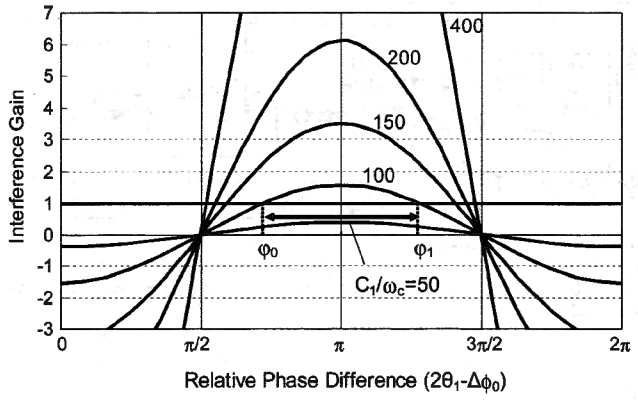


Fig. 3. Calculated interference gain versus the relative phase difference in a mesochronous system.

Then, the *interference gain* is defined using the above function as follows:

$$\text{Interference\_gain} \equiv \frac{\partial \left\| v_{X(\text{OUT})} \bullet \left(v_{X(\text{IN})} / v_{X0} \right) \right\|}{\partial v_{X0}}. \quad (19)$$

Under the condition $(C_{px}^{AB} \cdot C_{px}^{BA} \cdot \alpha_1^2)/(16) \cdot ((C_1)/(\omega_C))^2 \geqslant 1$, conditions I) and II) are modified as follows.

I) When interference gain $\geqslant 1$, a large amount of jitter may occur due to interference.

II) When interference gain < 1, the inherent phase noise is not enhanced by interference.

The calculated interference gain is shown in Fig. 3, where the following parameters are used:

$$C_{px}^{AB} \cdot \alpha_1 = C_{px}^{BA} \cdot \alpha_1 = 0.05$$
$$C_1/\omega_C = 50, 100, 150, 200, 400.$$

The following results are obtained.

- The interference gain is a sinusoidal function of the relative phase difference between the two PLL $(\Delta\phi_0)$.
- The peak value of the interference gain is approximately $(C_{px}^{AB} \cdot C_{px}^{BA} \cdot \alpha_1^2)/(16) \cdot ((C_1)/(\omega_C))^2$.
- The range from φ_0 to φ_1, in which the calculated interference gain is more than unity, does not exceed π [rad].

In mesochronous systems, the process of the enhancement of jitter generation is somewhat complicated. The interference gain depends on the relative phase difference $\Delta\phi_0$. When $\Delta\phi_0$ is set at a phase position where the system is under condition I), the inherent jitter may be enhanced to some extent. That causes the increase of the range of the relative phase difference. As the interference gain becomes larger, the system is thought to be unstable. Therefore, by increasing the range of the phase difference, a part of jitter may be enhanced more and it is possible that the system enters the unstable state where $\angle A(\Delta\omega) = 0$ and $A(\Delta\omega) \geqslant 1$. This enhancement process occurs when the increase of the amount of jitter is large enough under condition I). In fact, the calculation of the amount of jitter may require the introduction of nonlinear model.

In this paper, we employ the constant and real values as the coupling parameters C_{px}^{AB} and C_{px}^{BA}; however, the magnitude and phase of coupling between two adjacent circuits generally depends on the frequency of the noise signal. In order to deal with this issue, (10) should be rewritten using the complex number description

$$v_{n\_PD} = \alpha_1 \frac{v_{X0} \cdot C_1}{4\omega_C} \exp j(\omega_0 + \Delta\omega)t. \quad (20)$$

The coupling parameter can be expressed as follows:

$$C_{px}^{AB}(\omega) = \left| C_{px}^{AB}(\omega) \right| \cdot \exp j\theta^{AB}(\omega). \quad (21)$$

The voltage displacement of the adjacent VCO caused by the interference noise is given as follows:

$$v_{X,B} = \left| C_{px}^{AB}(\omega_0) \right| \cdot \alpha_1 \cdot \frac{v_{X0} \cdot C_1}{4\omega_C} \cdot \exp j[(\omega_0 + \Delta\omega)t + \theta^{AB}(\omega_0)]. \quad (22)$$

As a result, the interference noise by the other PLL in this case is obtained by the following replacements:

$$\theta_1 \rightarrow \theta_1 - \theta^{AB}(\omega_0) \quad \Delta\phi_0 \rightarrow \Delta\phi_0 + \theta^{BA}(\omega_0). \quad (23)$$

These changes shift the relative phase value where the interference gain becomes the maximum in Fig. 3.

Actually, there exist multiple interference paths between adjacent circuits, and the magnitudes and phases of coupling are different. Therefore, the total coupling parameter is written as follows:

$$C_{px}^{AB}(\omega) = \sum_k C_{px,k}^{AB}(\omega) \cdot \exp j\theta_k^{AB}(\omega). \quad (24)$$

Among the interference paths shown in (24), a large amount of jitter may occur whenever the interference gain satisfies condition I).

In this section, we introduced the ISF at the control node of a VCO and described the interference model in which the sideband noises from the carrier frequency interact with each other. Therefore, the instability in mesochronous systems is essentially a time-dependent phenomenon; in other words, the phenomenon is based on the LTV model.

We should note that this analysis is valid only when the ISF of VCO and the properties of the other elements of PLL hold the linearity. Moreover, since we employ the linear approximation in (8), the equations in the above analysis are correct, to be exact, when the perturbation into the loop filter is comparatively small. Our analysis predicts that a large amount of jitter may occur under condition I), but it can not be directly applied to the calculation of the amount of jitter. The amount of jitter under condition I) may be determined by the nonlinear model and equation that is beyond the scope of this paper.

C. Analysis of Interference Noise in Plesiochronous Systems

The previous method with regard to mesochronous systems can also be applied to the analysis of plesiochronous systems. Suppose the first PLL operates at ω_0 and the second at ω_1 with

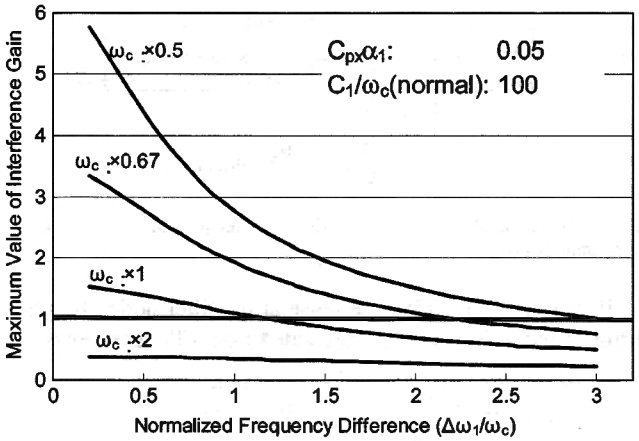


Fig. 4. Calculated peak value of interference gain versus the normalized frequency difference in a plesiochronous system.

the same noise injected to the loop filter, the phase error of the other PLL is given as follows:

$$\phi(t)^B = C_{px}^{AB} \cdot \alpha_1 \cdot \frac{v_{X0} \cdot C_1^2}{8\omega_C} \cdot f_\phi(\Delta\omega - \Delta\omega_1) \cdot \sin((\Delta\omega - \Delta\omega_1)t - \theta_1) \quad (25)$$

where $\Delta\omega_1 = \omega_1 - \omega_0$ and the ISF is expanded at ω_1. The function $f_\phi(\omega)$ is the closed-loop gain of the phase error. Based on PLL dynamics, $f_\phi(\omega)$ is derived as follows (see Appendix II):

$$f_\phi(\Delta\omega - \Delta\omega_1) \approx \frac{1}{\omega_C} \cdot \sqrt{\frac{1}{1 + ((\Delta\omega - \Delta\omega_1)/\omega_C)^2}}, \quad \text{where} \frac{\omega_n}{2\zeta} < \Delta\omega - \Delta\omega_1 < 2\zeta\omega_n. \quad (26)$$

By repeating the previous procedure, the output noise due to the coupling of the PLL is calculated as follows:

$$v_{X(\mathrm{OUT})} = C_{px}^{BA} \cdot \alpha_1 \cos\left[(\omega_0 + \Delta\omega_1)t + \frac{C_{px}^{AB} \cdot \alpha_1 \cdot v_{X0} \cdot C_1^2}{8\omega_C} \cdot f_\phi(\Delta\omega - \Delta\omega_1) \cdot \sin((\Delta\omega - \Delta\omega_1)t - \theta_1) + \Delta\phi_0\right]. \quad (27)$$

Fig. 4 shows the maximum value of the interference gain as a function of the frequency difference $\Delta\omega_1$. In the plesiochronous system, the relative phase difference $\Delta\phi_0$ may have an arbitrary value; therefore, the maximum value of the interference gain is just important to know whether the inherent noise is enhanced or not.

Note that the phase noise may increase due to interference in the frequency range in which the maximum interference gain exceeds unity. This analysis reveals the following results.

- With the decrease in the frequency difference between two oscillatory systems, the possible phase noise caused by the interference increases.
- The influence of the interference can be reduced by increasing the loop bandwidth of the PLL.

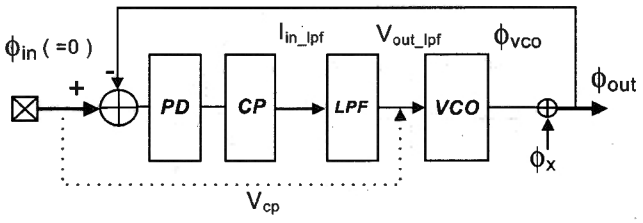


Fig. 5. Block diagram of the coupling noise of the reference signal into the loop filter in a PLL.

D. Analysis of Interference Noise in Synchronous Systems

In this section, we analyze the influence of the interference within a clock domain comprising one closed-loop system. Two types of interferences are discussed here: a direct disturbance of the reference signal into the loop filter and a direct coupling of the oscillator signal into the loop filter.

1) Analysis of Coupling of Reference Signal Into Loop Filter: Fig. 5 shows a model in which the coupling noise of the reference signal is introduced into the loop filter in a closed loop. It is possible that a large swing of the received reference signal may directly influence the loop filter or the control node of the internal oscillator via the substrate [14] or supply lines. In addition, the current variation in the receiver circuits may be one of the factors responsible for the coupling noise to the loop filter.

We shall investigate the response function from the input noise at the VCO to the output phase noise. First, we assume the input phase noise as

$$\phi_X \equiv \phi_{X0} \sin(\Delta\omega t). \quad (28)$$

The clock output can be expressed in the same manner as mentioned in Section II-B

$$V_{\mathrm{OUT}} \prec \cos(\omega_0 t + \phi_{X0} \sin(\Delta\omega t)) \cong \cos(\omega_0 t) + \frac{\phi_{X0}}{2}[\cos(\omega_0 + \Delta\omega)t - \cos(\omega_0 - \Delta\omega)t]. \quad (29)$$

In this paper, a multiplier is assumed to be a model of the phase detector [15] and the input reference signal is assumed to be an "ideal" signal, which implies that it has no external noise element.

The output of the phase detector $v_{\mathrm{out\_pd}}$ is given by

$$v_{\mathrm{out\_pd}} \cong \frac{k_{\mathrm{pd}}}{2} \sin\theta_{\mathrm{in}} + \frac{k_{\mathrm{pd}} \cdot \phi_{X0}}{4} \cdot [\sin(\theta_{\mathrm{in}} - \Delta\omega t) - \sin(\theta_{\mathrm{in}} + \Delta\omega t)] = \frac{k_{\mathrm{pd}}}{2} \sin\theta_{\mathrm{in}} - \frac{k_{\mathrm{pd}} \cdot \phi_{X0}}{2} \cos\theta_{\mathrm{in}} \sin(\Delta\omega t) \quad (30)$$

where k_{pd} is the gain of this phase detector and θ_{in} is the additional external phase error to this closed-loop system. In the lock state, the phase of the VCO output tracks the external phase input; this implies that θ_{in} becomes zero and the output of the detector becomes

$$v_{\mathrm{out\_pd}} = -\frac{k_{\mathrm{pd}} \cdot \phi_{X0}}{2} \sin(\Delta\omega t). \quad (31)$$

where we assume coupling with the ideal reference signal. θ_d is the delay in the coupling signal. The nonlinear term can be calculated using (35). The result obtained is as follows:

$$\begin{aligned} & v_{\text{out\_lpf\_NLR}} \\ &= \alpha_2 \cdot K_{\text{PD}} \cdot \phi_{X0} \sqrt{R^2 + (1/C\Delta\omega)^2} \cos(\Delta\omega t + \psi) \\ &\quad \cdot C_{px} \sin(\omega_0 t + \theta_{\text{in}} + \theta_d) \\ &= \frac{\alpha_2 \cdot K_{\text{PD}} \cdot C_{px} \cdot \phi_{X0}}{2} \sqrt{R^2 + (1/C\Delta\omega)^2} \\ &\quad \cdot [\sin((\omega_0 + \Delta\omega)t + \theta_{\text{in}} + \theta_d + \psi) \\ &\quad + \sin((\omega_0 - \Delta\omega)t + \theta_{\text{in}} + \theta_d - \psi)]. \end{aligned} \tag{42}$$

By applying this equation to the ISF of the VCO, the phase error of the VCO is represented as

$$\begin{aligned} & \phi_{\text{vco\_NLR}} \\ &= \frac{\alpha_2 \cdot K_{\text{PD}} \cdot C_{px} \cdot C_1 \cdot \phi_{X0}}{2} \sqrt{R^2 + (1/C\Delta\omega)^2} \\ &\quad \cdot \int \cos(\omega_0 t + \theta_1) \cdot [\sin((\omega_0 + \Delta\omega)t + \theta_{\text{in}} + \theta_d + \psi) \\ &\quad + \sin((\omega_0 - \Delta\omega)t + \theta_{\text{in}} + \theta_d - \psi)]\, dt. \end{aligned} \tag{43}$$

In the lock state, since $\theta_{\text{in}} = 0$, the phase error caused by the nonlinear term is simply written as

$$\begin{aligned} & \phi_{\text{vco\_NLR}} \\ &= \frac{\alpha_2 \cdot K_{\text{PD}} \cdot C_{px} \cdot C_1 \cdot \phi_{X0}}{2} \sqrt{R^2 + (1/C\Delta\omega)^2} \\ &\quad \cdot \frac{1}{\Delta\omega} \sin(\theta_d - \theta_1) \cdot \sin(\Delta\omega t + \psi). \end{aligned} \tag{44}$$

From (28), (37), and (44), when the nonlinearity effect of the unity gain buffer is considered, the total phase error of the VCO to the input signal at the control node in the loop filter is given as follows:

$$\begin{aligned} & \phi_{\text{vco\_tot}} \\ &\equiv \phi_{\text{vco}} + \phi_{vco\_NLR} \\ &= (1 - \beta) \cdot \frac{K_{\text{PD}} \cdot C_0 \cdot \phi_{X0}}{2} \sqrt{R^2 + (1/C\Delta\omega)^2} \\ &\quad \cdot \frac{1}{\Delta\omega} \sin(\Delta\omega t + \psi) \end{aligned} \tag{45}$$

where $\beta \equiv -\alpha_2 \cdot C_{px} \cdot (C_1/C_0) \sin(\theta_d - \theta_1)$.

In particular, when $\sin(\theta_d - \theta_1) < 0$ and $|\beta| \approx 1$, the open-loop gain in the low-frequency range can be controlled. As a result, in a PLL circuit, the nonlinear effect of the coupling noise of the reference signal into the loop filter may increase the sideband noise of the VCO. The sideband noise depends on the magnitude and the phase shift of the coupling noise of the reference signal.

Fig. 8 illustrates the nonlinear effect of the coupling of the reference signal by the linear equivalent model.[1] Note that in this case, we assume that $\sin(\theta_d - \theta_1) < 0$.

As shown in (45), the nonlinear effect of the coupling could include a variable β. The response function of the output of the phase error to the input signal at the VCO is expressed as

$$\frac{\phi_{\text{out}}}{\phi_{\text{in}}} = \frac{1}{1 + K_{\text{PD}} \cdot K_{\text{LF}}(s) \cdot (1 - \beta) \cdot \frac{K_v}{s}}. \tag{46}$$

[1]Note that Fig. 8 is inaccurate because it is based on the linear and time-invariant model. Fig. 8 can be interpreted as the quasi-linear model that takes into account of the nonlinear effect.

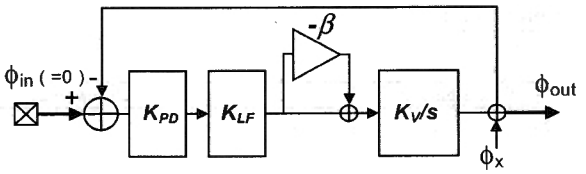


Fig. 8. Linear equivalent model of a PLL with the coupling noise of the reference signal into the loop filter.

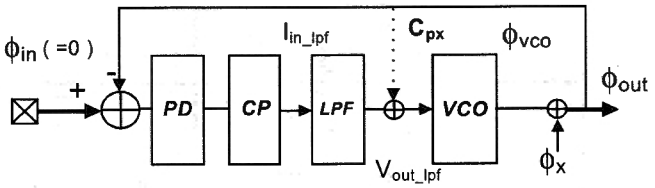


Fig. 9. Block diagram of the direct coupling of the clock output into the loop filter in a PLL.

This result implies that the open-loop gain reduces by a factor of $1-\beta$ as compared to that without the interference. Depending on the magnitude of coupling of the reference signal, the loop bandwidth of the PLL circuit may reduce considerably in comparison to the designed value.

2) Analysis of coupling from VCO to loop filter: Next, we present another example of coupling in a closed-loop system. Fig. 9 shows the model in which the output of the VCO is directly coupled into the loop filter. This situation may occur when the operational noise of the clock buffer is directly added to the control node of the VCO.

In this analysis, it is noteworthy that the influence of the phase error can be depicted without nonlinear terms. In other words, only the linear term of the coupling of the VCO output causes an unstable condition in the closed-loop system. The instability in the present closed-loop system under discussion may be more common than that in the previous case.

The clock output operates at a frequency of ω_0 and has a phase error of ϕ_{out}; therefore, the output of the loop filter in this model is a combination of the low-frequency element from the feedback loop and the high-frequency element from the coupling. The high-frequency element of the loop filter is down converted and it becomes the phase error of the VCO. We must consider the low- and high-frequency coefficients of the Fourier transfer in (1); we assume that C_{px} in Fig. 9 includes this effect.

In the linear equivalent model, the response of the output phase error ϕ_{out} for the input phase signal ϕ_x is expressed as

$$(\phi_{\text{out}}\phi_x = \phi_{\text{out}} \cdot \left[\left(1 + K_{\text{PD}} \cdot K_{\text{LF}}(s) \cdot \frac{K_v}{s}\right) - C_{px} \cdot \frac{K_v}{s}\right] \tag{47}$$

where we assume that the reference signal is ideal. The response function is derived as follows:

$$\frac{\phi_{\text{out}}}{\phi_{\text{in}}} = A(s) \cdot (1 - C_{px} \cdot B(s))^{-1} \tag{48}$$

where $A(s)$ and $B(s)$ are given as follows:

$$\begin{aligned} A(s) &\equiv \frac{1}{1 + K_{\text{PD}} \cdot K_{\text{LF}}(s) \cdot \frac{K_V}{s}} \\ B(s) &\equiv \frac{\frac{K_v}{s}}{1 + K_{\text{PD}} \cdot K_{\text{LF}}(s) \cdot \frac{K_v}{s}}. \end{aligned} \tag{49}$$

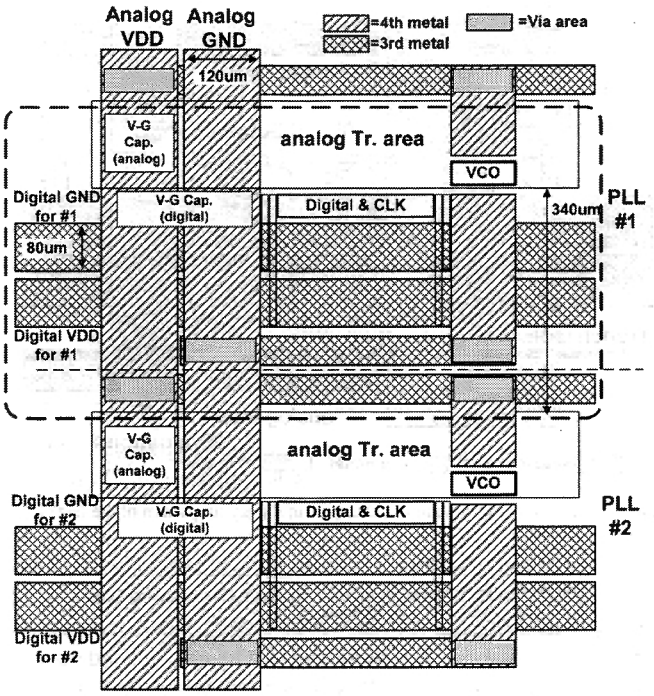


Fig. 11. Layout pattern of the two adjacent PLLs based on a test chip.

of digital circuits or current-mode logic. It seems that coupling reduction is the most effective method for controlling the phase error caused by interference.

In this section, we analyze the coupling via the supply lines and the substrate [9], [14], [20] by simulation and evaluate coupling reduction techniques.

A. Simulation of Coupling on Supply Lines Macromodel

Fig. 11 illustrates an example of the layout of the two adjacent PLL based on that of the test chip for the evaluation of mesochronous and plesiochronous systems. The features of this layout are as follows:

A) Analog transistor area includes circuits such as the VCO, charge pump, and loop filter. The digital block in this figure consists of the phase detector, flip-flop circuits, and the clock buffer.

B) Two closed-loop systems are contiguous with one side of the analog area of one PLL and the substrate of the digital circuits of the other PLL.

C) The distance between two PLL is around 450 um.

While carrying out the simulation of coupling via supply lines, we assume two types of supply line configurations: one involves two PLL sharing a single analog supply line and the other involves two PLL using the different analog supply lines.

As shown in Fig. 12, the signal level at the VCO circuit of PLL 2 is simulated when the charge is injected at the VCO circuit of PLL 1. According to the simulation results shown in Fig. 13, the coupling magnitude rages from − 14 dB to − 2 dB in the shared supply model. On the other hand, in the model involving different supply lines, the coupling magnitude is less than − 100 dB up to 10 MHz; however, this magnitude increases drastically in the high-frequency range and finally attains a value of more than − 30 dB at 1 GHz. The coupling magnitude in the

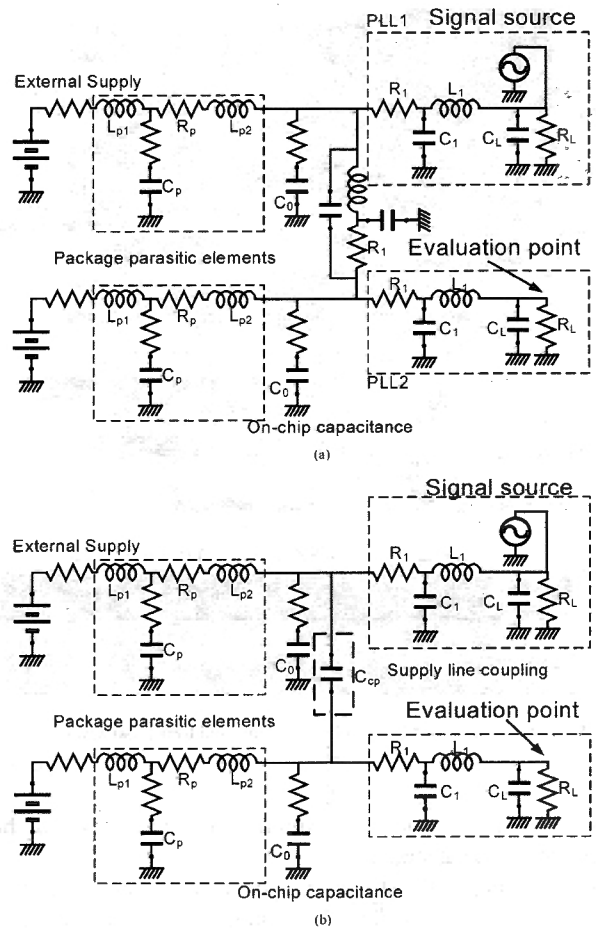


Fig. 12. Supply lines macromodels. (a) Shared analog supply model, (b) Different supply lines model.

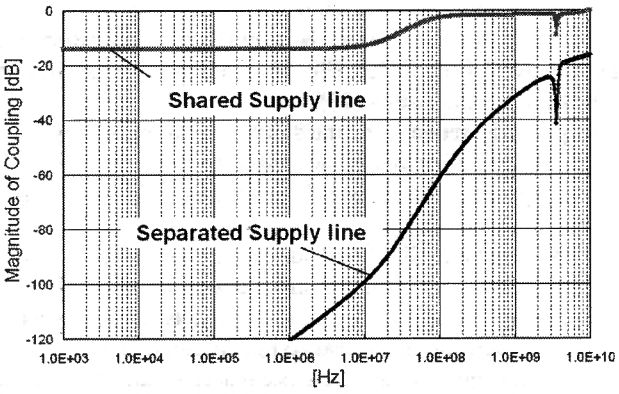


Fig. 13. Simulation results on supply lines macromodel.

high-frequency range is proportional to the parasitic capacitance C_{cp}, which is assumed as the inter-layer capacitance between supply lines. Therefore, in the case of a chip with multiple VCO circuits, the pattern of the supply lines as well as their separation must be considered carefully.

B. Resistive and Capacitive Network of Substrate Model

In order to estimate the coupling via substrate, we construct a resistive and capacitive network based on the layout of the test

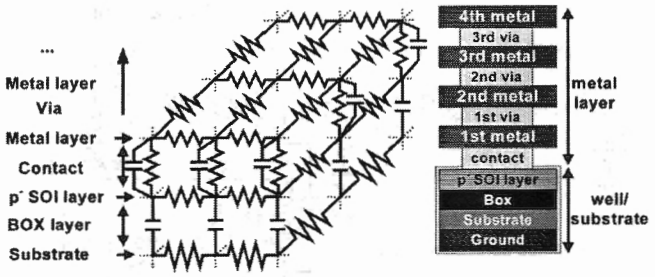


Fig. 14. Parasitic network model of the substrate and the supply line.

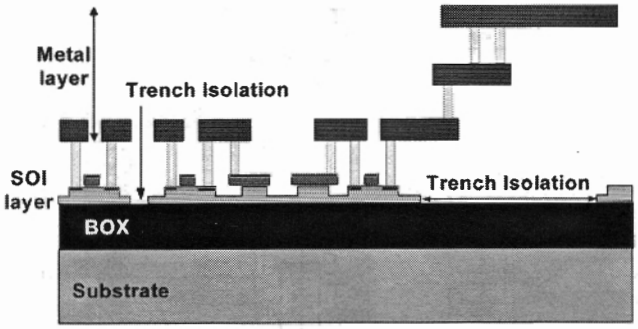


Fig. 15. Cross section of SOI/CMOS transistors and trench isolation.

chip mentioned previously and simulate the transmission of the noise signal via substrate.

Fig. 14 explains the structure of the resistive and capacitive network for the simulation of coupling via the substrate and supply line. Note that we adopt the silicon-on-insulator (SOI) structure in this simulation. The SOI-CMOS transistors have a high body resistance and the high-speed analog design should be carried out carefully [21]. However, one circuit can be easily isolated from another by trench isolation and the utilization of a high-resistive substrate [22]. Fig. 15 shows the cross section of the SOI CMOS transistors [22], [23].

The parasitic networks of the substrate and the supply lines are generated on the basis of the following rules.

A) The pattern of each layer is segmented into 5- to 40-μm square pieces.
B) The substrate, SOI layer, and each metal layer are constructed as equivalent resistive networks.
C) A group of via holes and gate contacts are represented as equivalent circuits that comprise resistive and capacitive elements. These elements connect a node of the upper layer to the corresponding node of the lower layer. In the absence of no via hole over 30-μm square units, the capacitive elements between layers are modeled.
D) The box layer and trench isolation area are modeled only as capacitive elements.[2]

The supply lines of the two PLLs are separated and each supply line is connected to the package parasitics and external supply line.

We have extracted the parasitic elements in the area bounded by broken lines in Fig. 11. The equivalent network of this model is composed of around 64500 passive elements, where the number of capacitive and resistive elements is 12500 and 52000, respectively.

[2]In fact, very large resistances are inserted in parallel with the capacitances to maintain a dc path for convergence in simulation.

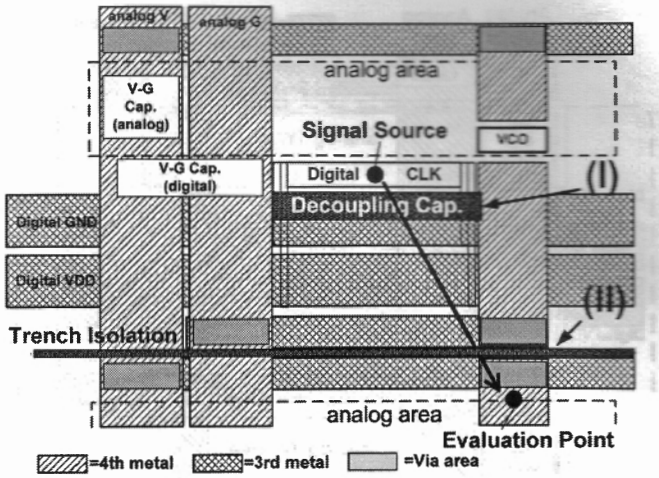


Fig. 16. Two kinds of isolation techniques in the layout pattern of the test chip.

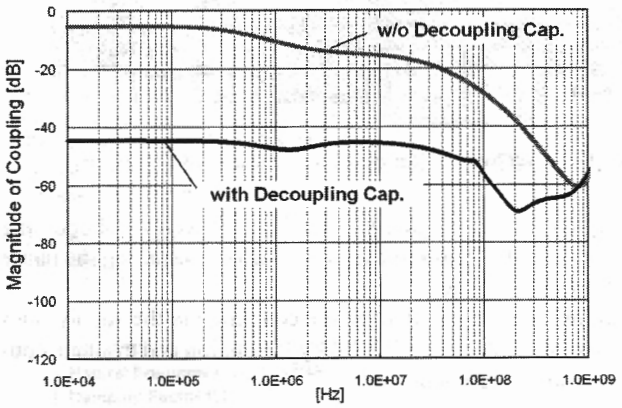


Fig. 17. Comparison of simulation results with or without decoupling capacitors at digital area.

C. Results of Coupling Simulation on Parasitic Network of Substrate

In order to verify the two types of isolation techniques, we compare the output signal magnitudes with or without isolations.

I) The decoupling capacitors between the digital supply and the ground are placed around the digital circuits, as shown in Fig. 16 [9]. Due to the decoupling capacitors based on MOS capacitors, the SOI layer of the digital block is well grounded and is expected to be immune to the operational noise in the digital block.
II) The trench isolation is placed on the boundary of the two PLL. The SOI layers of the two PLL are electrically disconnected from each other by the trench isolation.

Without any isolation, we found that the signal from the digital circuit transmits to the substrate of the analog area primarily via the SOI layer and the substrate. At around 100 kHz, the magnitude of transmission becomes more than -6 dB. However, as shown in Fig. 17, the transmission from the digital block to the

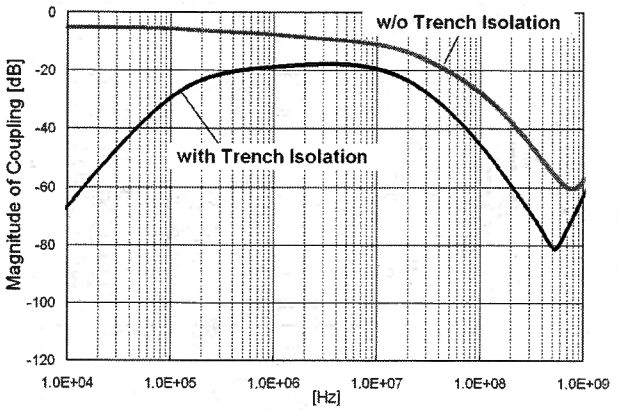


Fig. 18. Comparison of simulation results with or without trench isolation on boundary of analog and digital area.

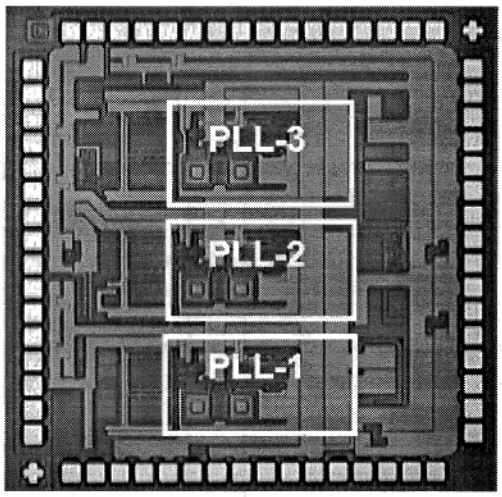


Fig. 19. Microphotograph of the test chip containing three clock recovery PLL.

analog area reduces significantly on the introduction of a decoupling capacitance. According to the simulation, the vale of the attenuation reaches 30 to 40 dB.[3] On the other hand, the low-frequency transmission of the operational noise is suppressed drastically by the trench isolation (Fig. 18). This effect seems to have degraded in the high-frequency ranges; however, the attenuation remains around 10 dB at several hundred megahertz.

IV. Experimental Results

In order to demonstrate and analyze the phenomena caused by the interference or coupling in oscillatory systems, the following experiments were carried out using test chips.

1) Measurement of the clock jitter while varying the relative phase difference and loop bandwidth of the PLL in a mesochronous system.
2) Measurement of the clock jitter while varying the frequency difference between two oscillators in a plesiochronous system.
3) Measurement of the dependency of the recovered clock jitter in a synchronous system on the amplitude of the reference signal.

A. Implementation of Test Chip

Fig. 19 shows a microphotograph of the test chip that was used for analyzing the interference noise between oscillatory systems. It consists of three clock recovery PLL and is fabricated using a 0.13-μm SOI-CMOS technology [24], [25]. The loop bandwidth of the clock recovery PLL with a linear phase detector is proportional to the transition density of the input data [26]–[28]; therefore, we can easily evaluate the dependency of the loop bandwidth of the PLL on the interference noise in oscillatory systems by changing the transition density of the received data. In this test chip, PLL 1 and PLL 2 share the same analog supply line, while PLL 3 has a different supply line. Moreover, the isolation techniques in the previous chapter are implemented between PLL 2 and PLL 3. These clock recovery PLL on the test chip can operate independent of each other. Thus, we can realize a mesochronous or plesiochronous system by varying the relative phase difference or frequency difference of incoming data among these oscillatory systems. In addition, we can verify the effect of the isolation technique by comparing the clock jitter generated when PLL 1 and PLL 2 operate with that generated when PLL 2 and PLL 3 operate.

[3]In the high-frequency range (greater than 1 GHz), the above mentioned transmission exhibits complex properties. One of the reasons may be the inaccurate package model; however, this will not be discussed.

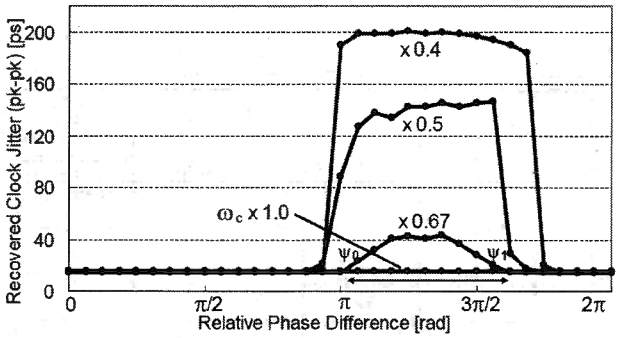


Fig. 20. Measured clock jitters versus the relative phase difference in a mesochronous system.

B. Measurement of Recovered Clock Jitter in Mesochronous Systems

We measured the jitter performance of the recovered clock of the PLL in mesochronous systems. Fig. 20 shows the measurement results; the X axis represents the relative phase difference between two adjacent PLL (PLL 1 and PLL 2) and the Y axis shows the peak-to-peak jitter of the recovery clock. We measured the loop bandwidth of the PLL by changing the transition density of the data. For example, if we define the loop bandwidth of the pseudorandom pattern or the "HHLL" pattern as unity, we can reduce the bandwidth to half by using the following input pattern: "HHHHLLLL." Fig. 20 also shows the measurement results for several input patterns. In these cases, when the loop bandwidth is less than two-third the unity bandwidth, the jitter caused by interference appears. As the loop bandwidth reduces, the interference causes an increase in the range of the relative phase difference in which the jitter occurs. The maximum range

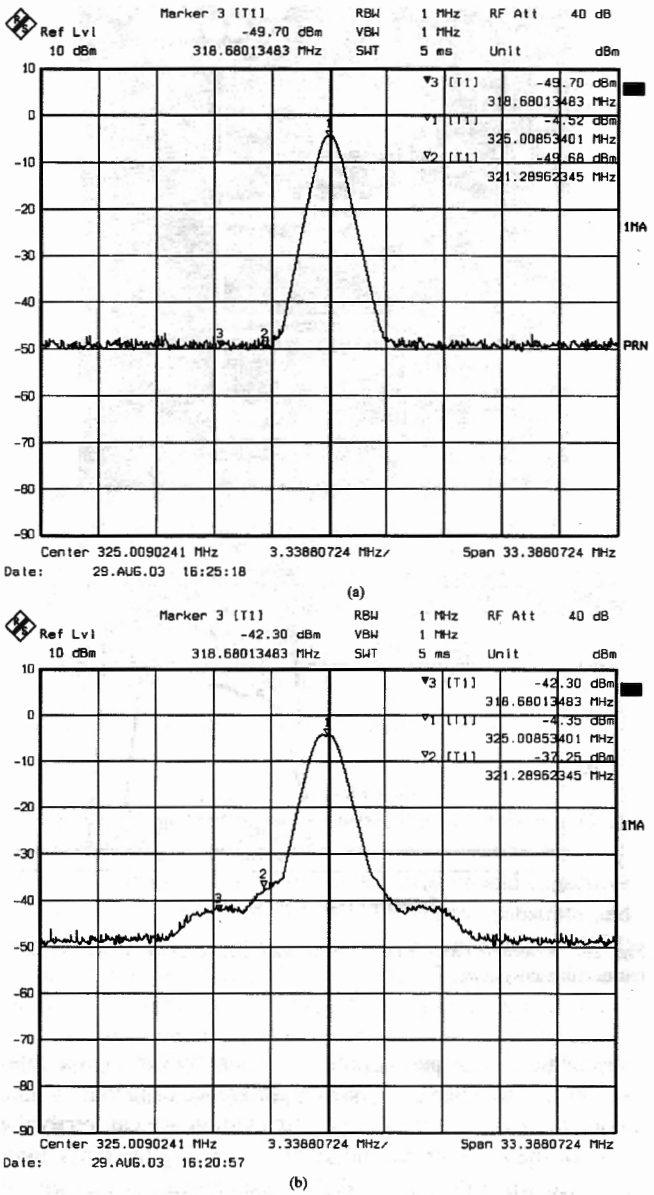


Fig. 21. Measured spectrums of the recovered clock (a) under the condition when the interference jitter does not appear, (b) under the condition when the interference jitter appears.

is approximately π [rad]. These results are consistent with a previous analysis conducted for mesochronous systems. However, the peak values of the measured jitters do not match those of the interference gain in Fig. 3, where the peak values are proportional to the square of the loop bandwidth. We believe that the phase error is strongly enhanced by positive feedback and that higher-order effects are dominant for jitter generation.

Fig. 21 shows the measured spectrums of the recovered clocks under two conditions: when the interference jitter appears and when it does not. It appears that the sideband noise whose frequency element is less than around 6 MHz increases when the interference jitter occurs.

We observe that when the two adjacent PLL have different supply lines and the substrates are well isolated, no jitter generation of the recovery clock is measured independent of the relative phase difference and the transition density of the data.

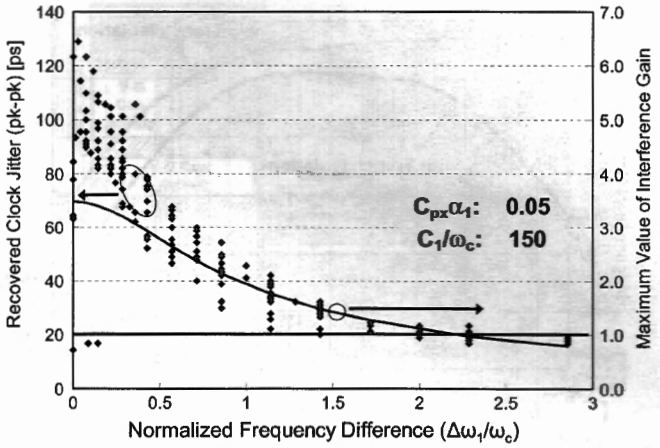


Fig. 22. Measured clock jitters and calculated maximum values of the interference gain in a plesiochronous system.

C. Measurement of Clock Jitter in Plesiochronous Systems

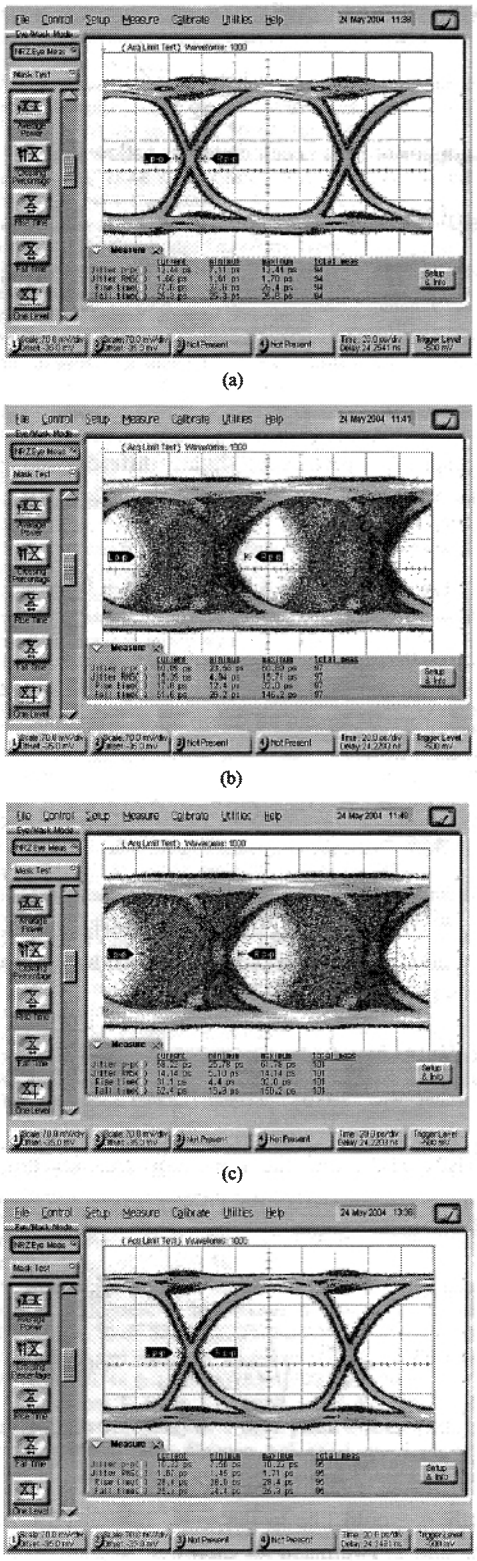
Next, we measured the recovered clock jitter in plesiochronous systems by changing the operation frequency of a PLL circuit (PLL 1) while maintaining a constant oscillation frequency of the adjacent PLL (PLL 2).

Fig. 22 shows the peak-to-peak jitters of the recovered clock at several center frequencies for three samples; X axis denotes the frequency difference normalized by the loop bandwidth. As the frequency difference between the two PLL reduces, the recovered clock jitter increases [29], [30]. The calculated maximum values of the interference gain shown in Fig. 4 are indicated on the solid line in Fig. 22. While we appropriately set the Y axis of the interference gain so as to match the measurement values, it appears that the jitter occurrence caused by the interference is strongly related to the maximum of the interference gain.

D. Occurrence and Control of Jitter caused by Coupling in Synchronous Systems

In order to evaluate the effect of the coupling in synchronous systems, we measured the recovered data eye patterns latched by the recovered clock in a clock recovery PLL with several amplitudes of the incoming data. The incoming data corresponds to the reference signal in a clock recovery PLL; therefore, if the coupling at the input port to the loop filter is dominant over the coupling from the reference to the loop filter, for example, via the substrate [14], the increase in the amplitude of the incoming data is equal to the increase in the coupling from the reference to the loop filter.

Fig. 23 shows the recovered data eyes for several amplitudes of the incoming data at the upper limit of the operation range. As shown in this figure, the jitter caused by the coupling can increase drastically when the magnitude of the incoming data amplitude exceeds a certain voltage level. In addition, according to the analysis in Section II-D, the jitter generation caused by coupling is related to the nonlinearity of the circuits connected to the loop filter. We compared the jitter at the middle of the frequency range with that at the upper limit of the range in



(a) (b) (c) (d)

Fig. 23. Recovered data eye patterns at the upper limit of the operation range with several amplitudes of the incoming data [(a), (b), (c)] and at the middle range with the same amplitude of the incoming data for comparison (d). (a) 125-mVpp differential. (b) 400-mVpp differential. (c) 1.0-Vpp differential. (d) 1.0-Vpp differential (middle of VCO range).

Fig. 23. Despite having the same incoming data amplitude, the latter is apparently larger than the former. This is because the linearity of the unity gain buffer that controls the VCO would degrade at the upper limit of the operation range and the clock buffer would be sensitive to external noise. From the previous analysis, it is inferred that this type of jitter generation arises from a limitation in the bandwidth of the PLL due to coupling; therefore, we observed the relationship between the jitter generation and the loop bandwidth of the PLL. In the measurement of mesochronous systems, we changed the transition density of the incoming data in order to change the loop bandwidth of the PLL; however, in this case, the coupling parameter from the reference is also a function of the transition density of the incoming data. Then, we changed the loop bandwidth by changing the values of the passive element of the loop filter. Fig. 24 illustrates the measured eye diagrams in which the loop bandwidths are greater than the designed value by factors of 1.0, 1.5, 2.0, and 3.5. It is observed that the jitter generation caused by the coupling can be controlled by increasing the bandwidth of the PLL. These results are consistent with those of the previous analysis.

V. Conclusion

This paper provides new insight into the interference and coupling phenomena in synchronous systems. From this analysis, we first revealed that a small perturbation to an oscillator can be enhanced by positive feedback through coupling with another oscillatory system. This implies that the inherent phase error caused by thermal noise can lead to a large amount of jitter due to interference without any external noise. The analysis also reveals the relationship between the frequency difference in a plesiochronous system and the occurrence of the large amount of jitter. In addition, we showed that the coupling noise within a closed-loop system with one oscillator can lead to the limitations in the bandwidth of the PLL and the peak gain of the response of the phase error of the clock, which may lead to the large amount of jitter.

We evaluated these phenomena by conducting measurements on test chips. We confirmed that the occurrences of jitter caused by interference in mesochronous and plesiochronous systems were consistent with the prediction of the analysis. We also evaluated the jitter generation caused by coupling from the reference to the loop filter. We observed that this jitter generation could be controlled by increasing the bandwidth of the PLL.

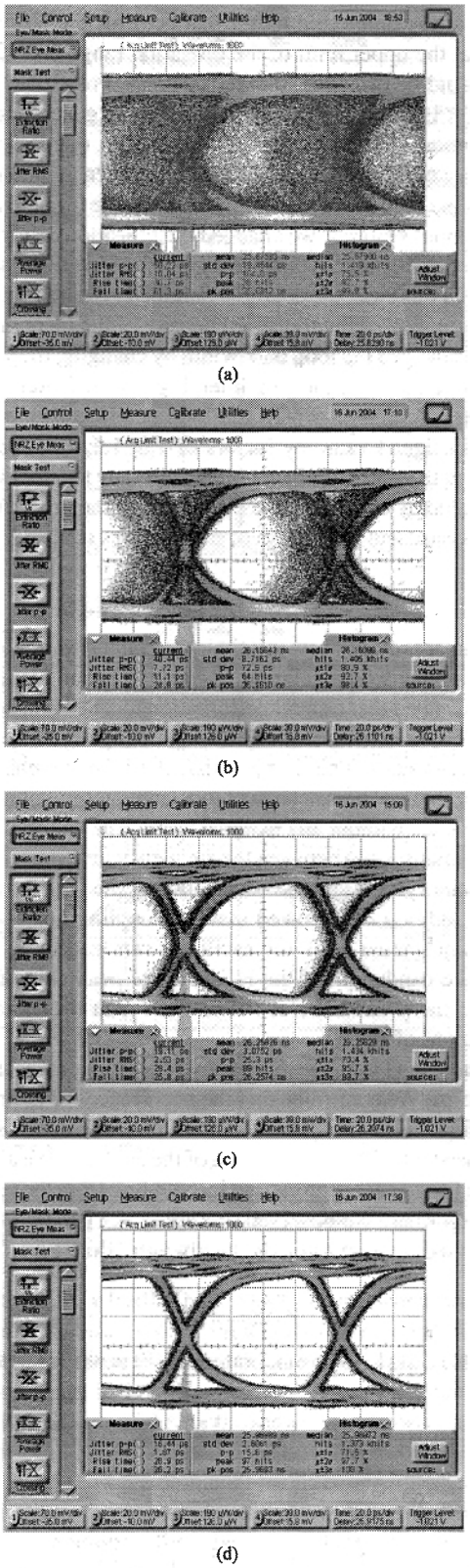
Appendix I

From (4) and (13), the numerator of (18) is written as follows:

$$\int^{t} v_{X(\mathrm{OUT})}(\tau)\cdot\left(v_{X(\mathrm{IN})}(\tau)/v_{X0}\right)d\tau = \int^{t} C_{px}^{BA}\alpha_1 \times\cos\left[\omega_0\tau+\frac{C_{px}^{AB}\alpha_1 v_{X0}}{8}\left(\frac{C_1}{\omega_c}\right)^2\sin(\Delta\omega\tau-\theta_1)+\Delta\phi_0\right]\cdot\cos\left[(\omega_0+\Delta\omega)\tau+\theta_1\right]d\tau. \quad \text{(A1)}$$

Now, we use the following trigonometric identities:

$$\cos X\cdot\cos Y=\frac{\cos(X+Y)+\cos(X-Y)}{2}. \quad \text{(A2)}$$



(a) (b) (c) (d)

Fig. 24. Dependency of loop bandwidths of PLLs on the peak-to-peak jitter of recovered data eye patterns. (a) 1.0 times the designed value. (b) 1.5 times the designed value. (c) 2.0 times the designed value. (d) 3.5 times the designed value.

By setting $X = (\omega_0 + \Delta\omega)\tau + \theta_1$ and $Y = \omega_0\tau + (C_{px}{}^{AB}\alpha_1 v_{X0}/8)(C_1/\omega_c)^2 \sin(\Delta\omega\tau - \theta_1) + \Delta\phi_0$, we can derive the numerator of (18).

From the following identity:

$$\cos^2 Z = \frac{1+\cos 2Z}{2} \tag{A3}$$

the denominator of (18) is calculated as follows:

$$\int^t \left(v_{X(\mathrm{IN})}(\tau)/v_{X0}\right)^2 d\tau = \frac{1}{2} \times \int^t [1+\cos(2(\omega_0+\Delta\omega)\tau + 2\theta_1)]d\tau \sim \frac{1}{2}t \tag{A4}$$

when $t >> (2\pi/2(\omega_0 + \Delta\omega))$.

Appendix II

We can also use (4) to (11) for a plesiochronous system. Next, since the other PLL operates at a slightly different frequency ω_1, the impulse sensitivity function can be expanded as

$$\Gamma_B \equiv \frac{C_0^B}{2} + \sum_k C_k^B \cos\left(k\omega_1 t + \theta_k^B\right). \tag{B1}$$

We assume that the coefficients of the Fourier series of ISF for one VCO are identical to those for the other VCO. The phase error of the other VCO can be obtained in a manner similar to that in (5) as follows:

$$\phi(t)^B_{\mathrm{open}} = \int^t v_X^B \cdot \Gamma_B d\tau \approx C_{px}^{AB}\alpha_1 \frac{v_{X0}\cdot C_1^2}{8\omega_c} \cdot \frac{1}{\Delta\omega - \Delta\omega_1}\sin((\Delta\omega - \Delta\omega_1)t_1). \tag{B2}$$

When $\omega > (\omega_n/2\zeta)$, the closed-loop transfer function from an additive noise on the VCO control voltage to the phase error is shown as [14]

$$H_v(s) = \frac{sK_0}{s^2 + 2\zeta\omega_n s + \omega_n^2} \approx \frac{K_0}{s + 2\zeta\omega_n} = \frac{K_0}{s+\omega_C}. \tag{B3}$$

From (B2), (B3), and the open-loop transfer function of VCO:(K_0/s), we can derive the phase error of the closed loop in a plesiochronous system as follows:

$$\phi(t)^B_{\mathrm{close}} \equiv \phi(t)^B = \left|\frac{H_v}{K_0/s}\right| \cdot \phi(t)^B_{\mathrm{open}} = \frac{|s|}{\omega_C}\cdot\sqrt{\frac{1}{(s/\omega_C)^2+1}}\cdot\phi(t)^B_{\mathrm{open}}. \tag{B4}$$

By substituting $\Delta\omega - \Delta\omega_1$ into s in (B4), we can obtain (25).

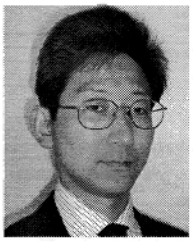
Acknowledgment

The authors would like to thank K. Takata, H. Kondoh, S. Yamauchi, and T. Iwamatsu for their help and support.

References

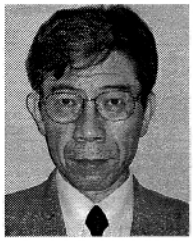
[1] B. Razavi, "A study of injection locking and pulling in oscillators," *IEEE J. Solid-State Circuits*, vol. 39, no. 9, pp. 1415–1424, Sep. 2004.
[2] A. Hajimiri and T. H. Lee, "A general theory of phase noise in electrical oscillators," *IEEE J. Solid-State Circuits*, vol. 33, no. 2, pp. 179–194, Feb. 1998.
[3] B. Razavi, "A study of phase noise in CMOS oscillators," *IEEE J. Solid-State Circuits*, vol. 31, no. 3, pp. 331–343, Mar. 1996.

[4] A. Demir, A. Mehrotra, and J. Roychowdhury, "Phase noise and timing jitter in oscillators," in *Proc. Custom Integr. Circuits Conf.*, , May 1998, pp. 4.2.1–4.2.4..
[5] F. Herzel and B. Razavi, "A study of oscillator jitter due to supply and substrate noise," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 46, no. 1, pp. 56–62, Jan. 1999.
[6] P. Heydari, "Analysis of the PLL jitter due to power/ground and substrate noise," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 51, no. 12, pp. 2404–2416, Dec. 2004.
[7] W. J. Dally and J. W. Poulton, *Digital Systems Engineering*. Cambridge, U.K.: Cambridge University Press, 1998, ch. 10.
[8] T. Yoshimura and A. Iwata, "An analysis of interference in synchronous systems," *IEICE Electronics Express (ELEX)*, vol. 1, no. 15, pp. 465–471, Nov. 2004.
[9] M. Nagata, J. Nagai, K. Hijikawa, T. Morie, and A. Iwata, "Physical design guides for substrate noise reduction in CMOS digital circuits," *IEEE J. Solid-State Circuits*, vol. 36, no. 3, pp. 539–549, Mar. 2001.
[10] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*. New York: Cambridge University Press, 1998, ch. 17.
[11] T. Yoshimura, "A Study of Interface Circuits for High-Speed Serial Data Links (in Japanese)," Ph.D. dissertation, Dept. Elect. Eng., Hiroshima Univ., Hiroshima, Japan, 2005.
[12] W. F. Egan, *Phase-Lock Basics*. New York: Wiley, 1998, ch. 11.
[13] P. R. Gray and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*. New York: Wiley, 1977, ch. 9.
[14] B. E. Owens, S. Adluri, P. Birrer, R. Shreeve, S. K. Arunachalam, K. Mayaram, and T. S. Fiez, "Simulation and measurement of supply and substrate noise in mixed-signal ics," *IEEE J. Solid-State Circuits*, vol. 40, no. 2, pp. 382–391, Feb. 2005.
[15] B. Razavi, Ed., *Monolithic Phase-Locked Loops and Clock and Data Recovery Circuits*. New York: IEEE Press, 1996, in Tutorial.
[16] F. M. Gardner, "Charge-pump phase-locked loops," *IEEE Trans. Commun.*, pp. 1849–1858, Nov. 1980.
[17] R. E. Best, *Phase-Locked Loops*. New York: McGraw-Hill, 1993, ch. 2.
[18] W. B. Wilson, U. K. Moon, K. R. Lakshmikumar, and L. Dai, "A CMOS self-calibrating frequency synthesizer," *IEEE J. Solid-State Circuits*, vol. 35, no. 10, pp. 1437–1444, Oct. 2000.
[19] S. Dosho and N. Yanagisawa, "A background Optimization method for PLL by measuring phase jitter performance," in *Dig. Tech. Papers Symp. VLSI Circuits*, 2004, pp. 236–239.
[20] A. Samavedam, A. Sadate, K. Mayaram, and T. S. Fiez, "A scalable noise coupling model for design of mixed-signal ICs," *IEEE J. Solid-State Circuits*, vol. 35, no. 6, pp. 895–904, Jun. 2000.
[21] K. Chang, S. Pamarti, K. Kaviani, E. Alon, X. Shi, T. J. Chin, J. Shen, G. Yip, C. Madden, R. Schmitt, C. Yuan, F. Assaderaghi, and M. Horowitz, "Clocking and circuit design for a parallel I/O on a first-generation CELL processor," in *Dig. Tech. Papers ISSCC'05*, Feb. 2005, pp. 526–527.
[22] S. Maeda, Y. Wada, K. Yamamoto, H. Komurasaki, T. Matsumoto, Y. Hirano, T. Iwamatsu, Y. Yamaguchi, T. Ipposhi, K. Mashiko, S. Maegawa, and M. Inuishi, "Feasibility of 0.18-μm SOI CMOS technology using hybrid trench isolation with high resistivity substrate for embedded RF/analog application," *IEEE Trans. Electron Devices*, vol. 48, no. 9, pp. 2065–2073, Sep. 2001.
[23] Y. Hirano, S. Maeda, T. Matsumoto, K. Nii, T. Iwamatsu, Y. Yamaguchi, T. Ipposhi, H. Kawashima, S. Maegawa, M. Inuishi, and T. Nishimura, "Bulk-layout-compatible 0.18-μm SOI-CMOS technology using body-tied partial-trench-isolation (PTI)," *IEEE Trans. Electron Devices*, vol. 48, no. 12, pp. 2816–2822, Dec. 2001.
[24] T. Yoshimura, K. Ueda, J. Takasoh, and H. Kondoh, "A 10 gbase ethernet transceiver (LAN PHY) in a 1.8 V, 0.18-μm SOI/CMOS technology," *IEICE Trans. Electron.*, vol. E86-C, no. 4, pp. 643–651, Apr. 2003.
[25] J. Takasoh, T. Yoshimura, H. Kondoh, and N. Higashisaka, "A 12.5 Gbps half-rate CMOS CDR circuits for 10 Gbps network applications," in *Dig. Tech. Papers Symp. VLSI Circuits*, 2004, pp. 268–271.
[26] R. C. Waker, C. L. Stout, J. T. Wu, B. Lai, C. S. Yen, and T. Hornak, "A two-chip 1.5-GBd serial link interface," *IEEE J. Solid-State Circuits*, vol. 27, no. 12, pp. 1805–1811, Dec. 1992.
[27] Y. M. Greshishchev and P. Schvan, "SiGe clock and data recovery IC with linear-type PLL for 10-Gb/s SONET application," *IEEE J. Solid-State Circuits*, vol. 35, no. 9, pp. 1353–1359, Sep. 2000.
[28] H. Nosaka, K. Ishii, T. Enoki, and T. Shibata, "A 10-Gb/s data-pattern independent clock and data recovery circuit with a two-mode phase comparator," *IEEE J. Solid-State Circuits*, vol. 38, no. 2, pp. 192–197, Feb. 2003.
[29] I. Fujimori, "CMOS LSIs for optical communications: 10 Gb/s technology and future directions," presented at the Fiber Optics Expo (FOE) Tech. Conf., Jan. 22, 2003, unpublished.
[30] A. L. Coban, M. H. Koroglu, and K. A. Ahmed, "A 2.5–3.125-Gb/s quad transceiver with second-order analog DLL-based CDRs," *IEEE J. Solid-State Circuits*, vol. 40, no. 9, pp. 1940–1947, Sep. 2005.



Tsutomu Yoshimura (M'05) received the B.S. and M.S. degrees in physics from the University of Tokyo, Tokyo, Japan, in 1989 and 1991, respectively, and the Ph.D. degree in electrical engineering from Hiroshima University, Hiroshima, Japan, in 2005.

Since 1993, he has been with Mitsubishi Electric Corporation, Itami, Japan, where he contributed toward the design of system LSIs for optical communication systems. From 2001 to 2004, he worked on the design of integrated circuits for a 10-Gbase ethernet transceiver large-scale integration. Since 2005, he has been engaged in the design of fully integrated optical transceivers. His interests are the design of high-speed analog and digital circuits, including a phase-locked loop, a clock recovery circuit, and the equalizer for backplane applications. He is also interested in researching interference and coupling between closed-loop systems.



Atsushi Iwata (M'87) received the B.E., M.S., and Ph.D. degrees in electronics engineering from Nagoya University, Nagoya, Japan, in 1968, 1970, and 1994, respectively.

From 1970 to 1993, he was with the Electrical Communications Laboratories, Nippon Telegraph and Telephone Corporation, Kanagawa, Japan. Since 1994, he has been a Professor of Electrical Engineering at Hiroshima University, Hiroshima, Japan. His research is in the field of integrated circuit design where his interests have included circuit architecture and design techniques for analog-digital mixed large-scale integrations (LSIs), wireless interconnections, substrate noise reduction, three-dimensional (3-D) integrated image processors, and bio-inspired signal processing LSIs. He was the Program Chairman for the 1995 Symposium on VLSI Circuits and the Chairman for the 1999 Symposium on VLSI Circuits.

Prof. Iwata has been an Associate Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS. He received an Outstanding Panelist Award for the 1990 International Solid-State Circuits Conference. He is a member of the Institute of Electronics, Information and Communication Engineer and the Japanese Neural Network Society.