The Architecture of Delta Sigma Analog-to-Digital Converters Using a Voltage-Controlled Oscillator as a Multibit Quantizer

Atsushi Iwata, Noboru Sakimura, Makoto Nagata, and Takashi Morie

Abstract— **This brief proposes a new architecture for the oversampling delta–sigma analog-to-digital converter (ADC) utilizing a voltage-controlled oscillator (VCO). The VCO, associated with a pulse counter, works as a high-speed quantizer. This VCO quantizer also has the function of first-order noise shaping because the phase of the output pulse is an integrated quantity of the input voltage. If the maximum VCO frequency (fvm) is designed in the range of $(2^{bq}-2)fos < fvm < (2^{bq}-1)fos$ and a *bq*-bit counter is used, a multibit (*bq*-bit) quantizer can be realized, where fos is the oversampling frequency. The performance of the proposed converter is evaluated using a functional simulation. A 59-dB SNR at a 5-MHz bandwidth is obtained with $fos = 400$ MHz, even in the case of a 1-bit quantizer. The multibit quantizer using a high-frequency VCO significantly improves an SNR and signal bandwidth. This architecture is highly suitable for implementation with deep sub-μm CMOS devices, which can attain improved switching speeds and reduce power dissipation during low voltage operation. It provides wideband oversampling ADC for video and wireless signals and a low voltage system-on-a-chip solution for multimedia applications.**

Index Terms— **Multibit quantizer, noise shaping, oversampling delta–sigma A–D converter, voltage-controlled oscillator.**

I. Introduction

Throughout the last decade, oversampling delta–sigma modulation techniques were intensively studied to develop a high-accuracy analog-to-digital converter (ADC) for voice and audio applications [1]. It has become the primary technique for sub-μm CMOS analog-to-digital mixed-signal large-scale integrations (LSI's), because the analog parts of the converter are very simple and the required accuracy is relatively low. It also allows the use of digital filters for eliminating alias noise and shaped quantization noise, which can be integrated with scaled CMOS technologies with low power and small area.

The purpose of our research is to expand the bandwidth of an oversampling ADC to the 1-MHz range, and to develop application areas for video and wireless communication signal processing. The first approach for extending the signal bandwidth (fb) is to increase the oversampling frequency (fos). As an example of this approach, a bipolar delta–sigma modulation chip with a 1.28-GHz oversampling frequency (fos) was reported. However, it consumed a large power of 250 mW with a 5-V supply [2]. The approach of increasing fos is not easy because it is limited by device performance and power dissipation.

If fb is enlarged with a limited fos, a signal-to-noise ration (SNR) degrades due to the decrease of oversampling ratio ($fos/2fb$). The approach to solving this problem is to increase the quantizer resolution or the order of noise-shaping filters. Existing multibit quantization architectures need a large number of devices and substantial dissipation power, because a flash ADC and a highly linear feedback

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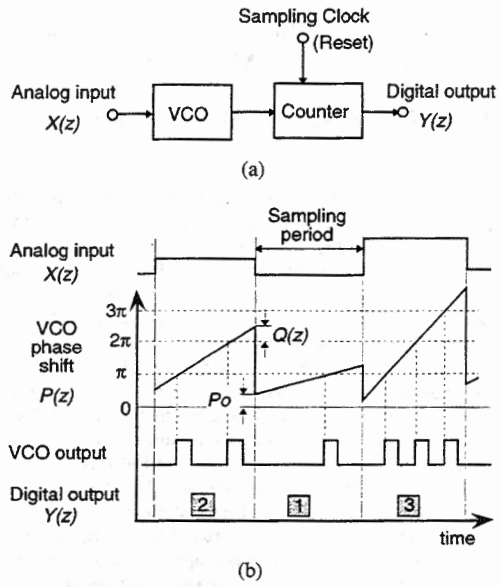

Fig. 1. VCO Quantizer. (a) Block diagram of VCO quantizer. (b) Operation principle and waveforms.

digital-to-analog converter (DAC) are required [3]. Higher order noise-shaping architecture generally has stability problems which limit SNR performance. Several techniques to prevent oscillation, such as multistage noise shaping (MASH), have been proposed [4].

Our approach is quite different from these ordinary delta–sigma techniques. It utilizes time domain information such as pulse width, phase, and frequency [5], [6]. This time-domain information can be processed by deep sub-μm CMOS devices operated at lower supply voltage and with lower power dissipation than achievable by ordinary analog circuit techniques.

II. Architecture

The key circuit for time-domain analog processing is a voltage-controlled oscillator (VCO). A VCO operates as a logic circuit in the voltage domain because it generates binary pulses. But it works as an analog circuit for voltage-to-time conversion in the time domain, because the output pulse frequency is controlled by the analog input voltage. The proposed architecture utilizes a VCO as a quantizer. The behavior of the VCO quantizer is analyzed using z transfer functions characterized with a sampling clock of fos. It consists of a VCO and a binary counter with a reset, as shown in Fig. 1(a). The VCO generates pulses when its internal phase value reaches the value of $2\pi n$, where n is an integer, as shown in Fig. 1(b). The internal phase shift of $P(z)$ is proportional to an input voltage of $X(z)$. Assuming G_v is a gain constant and P_o is an initial phase

$$P(z) = G_v X(z) + P_o. \tag{1}$$

The VCO output pulses are counted during a sampling period $1/fos$, where the counter is reset following each sampling period. The count of $Y(z)$ is a quantized value for $P(z)$. A residual phase shift at the end of the sampling period is quantization noise $Q(z)$

$$Q(z) = P(z) - 2\pi Y(z). \tag{2}$$

$Q(z)$ is held to be the initial phase shift for the next sampling period.

$$P_o = z^{-1}Q(z). \tag{3}$$

From (1)–(3), transfer characteristics of the VCO quantizer are obtained

$$Y(z) = (1/2\pi)[G_v X(z) + (1 - z^{-1})Q(z)]. \tag{4}$$

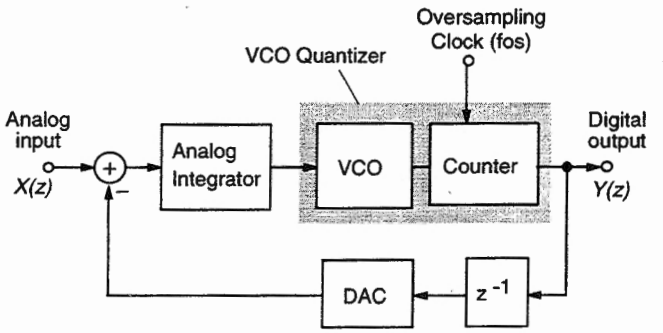

Fig. 2. Block diagram of VCO-DS-ADC.

Equation (4) shows that quantization noise $Q(z)$ is shaped by a first-order high-pass filter. Therefore, the VCO quantizer has the function of a first order delta–sigma ADC.

If the VCO frequency is designed not to exceed the sampling frequency, the count of $Y(z)$ is "0" or "1", and the quantizer resolution is 1 bit. In this case, because the oversampling frequency (fos) is approximately equal to the maximum frequency of the VCO (fvm), a high-speed quantizer with $fos > 500$ MHz is easily realized with sub-μm CMOS technologies. If the maximum VCO frequency (fvm) is in the range of $(2^{bq} - 2)fos < fvm < (2^{bq} - 1)fos$ and the bit of counter is bq (=2, 3, $\cdots$), a multibit (bq-bit) quantizer can be realized.

The proposed delta–sigma ADC utilizes the VCO quantizer as shown in Fig. 2. It is called VCO-digital signal (DS)-ADC. A first-order analog integrator is added before the VCO quantizer. If an ideal integrator is used, transfer characteristics of the converter is given as follows:

$$Y(z) = (1/2\pi)[G_v X(z) + (1 - z^{-1})^2 Q(z)]. \tag{5}$$

This equation shows that the proposed VCO-DS-ADC has second-order noise-shaping characteristics. Using the multibit quantizer and feedback DAC, SNR performance is improved. The theoretical SNR of the multibit VCO-DS-ADC is calculated by the same method as the conventional DS-ADC.

The noise power of the second-order DS-ADC is $P_e = \Delta^2\pi^4/60M^5$, and the ac power of the sinusoidal wave is $P_s = \Delta^2 2^{2bq}/8$, where Δ is the quantization level spacing, M is the oversampling ratio ($fos/2fb$), and bq is the quantizer resolution. Therefore, maximum SNR is given by

$$\text{SNR max (dB)} = 50\log M + 6.02\text{bq} - 11.1. \tag{6}$$

In VCO-DS-ADC, the maximum input signal swing is $(2^{bq}-1)\Delta$ and the noise power is the same as the conventional DS-ADC. Therefore, a maximum SNR is given by

$$\text{SNR max (dB)} = 50\log M + 20\log(2^{bq} - 1) - 17.2. \tag{7}$$

Basic operation of the proposed VCO-DS-ADC was confirmed and SNR performance was evaluated by the discrete time-functional simulator for digital signal processing (SPW). To simulate a continuous-time analog integrator, it was approximated by multiplying the simulation system clock and dividing the sampling period by 5–8. The simulated waveforms of various nodes are shown in Fig. 3.

III. Circuit Configuration

The voltage-to-frequency conversion gain of the VCO should increase as much as possible, because it determines the gain of the delta–sigma loop. A CMOS VCO with a ring oscillator was designed using differential variable-delay cells, as shown in Fig. 4.

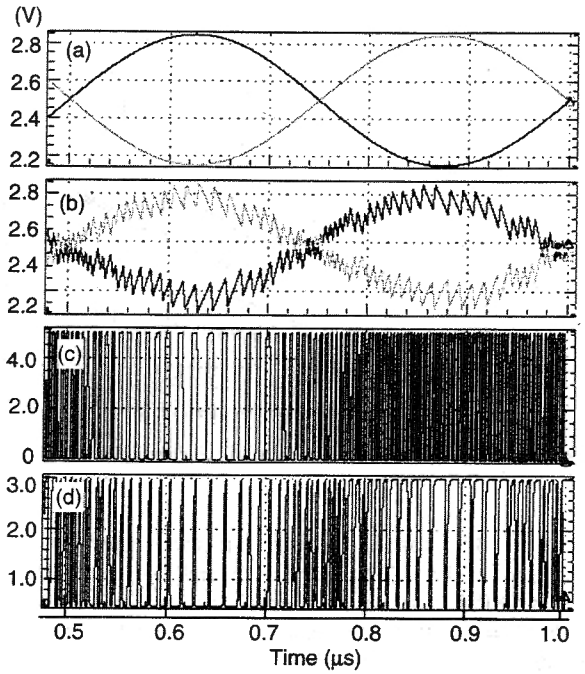

Fig. 3. Simulated waveforms of VCO-DS-ADC.(a) Analog inputs. (b) Integrator outputs. (c) VCO output. (d) Digital output (PDM signal with an open drain).

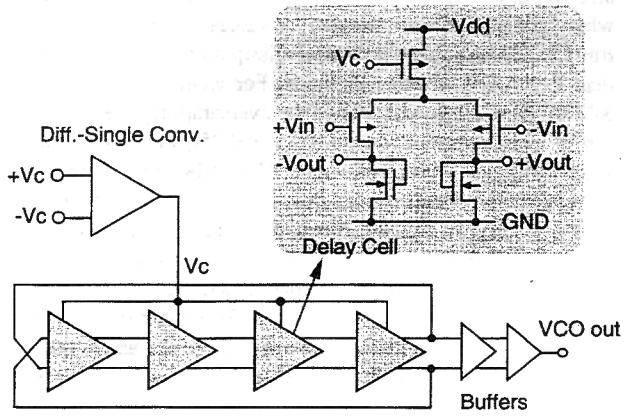

Fig. 4. Circuit schematic of CMOS VCO using differential delay circuits.

The differential circuit configuration is necessary to obtain low jitter characteristics against power-supply noise and substrate noise. A maximum frequency of 400 MHz was obtained with a 0.6-μm CMOS operating at a 3.3-V supply voltage. High linearity of the conversion gain is also required because it affects SNR characteristics. The simulated nonlinearity was as low as 1.3% within an input range of -0.5 to 0.5 V as shown in Fig. 5.

The analog integrator for noise shaping can be implemented with an *RC* circuit or a *gm-C* circuit. The former is simple and works with low power dissipation, but it does not provide a gain, even in a low-frequency range. Noise-shaping characteristics suffer from the saturation of the integrator gain at low frequencies because the loop gain does not increase. The latter provides the better integration characteristics of high gain at low frequency, although it consumes larger power than the *RC* approach.

In order to feedback the quantized values to the analog integrator, a high-speed DAC which operates at the oversampling frequency (fos) is required. For the DAC, sufficiently high linearity is required because its nonlinearity causes harmonic distortions and degrades

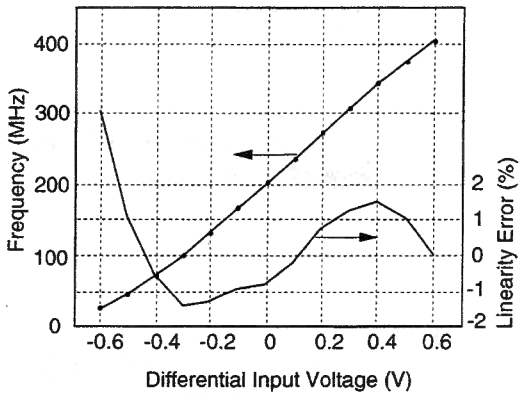

Fig. 5. Voltage-to-frequency conversion gain and its linearity of the CMOS VCO.

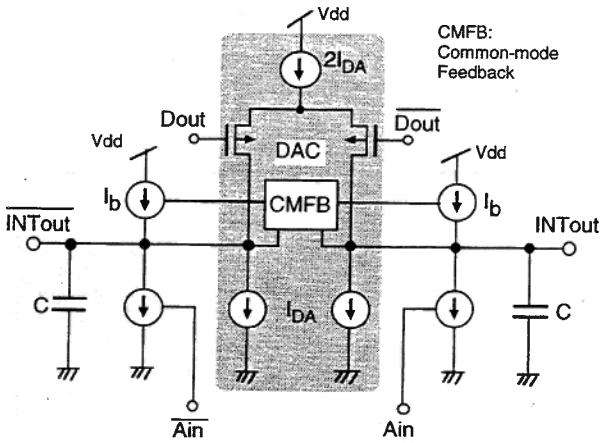

Fig. 6. Circuit schematic of the *gm-C* integrator and feedback DAC.

SNR. To obtain the high linearity, a 1-bit DAC which has only two output levels and inherent linearity should be used, even if a multibit quantizer is used. To reduce the bit of feedback to 1 bit, the multibit quantizer outputs are requantized by digital processing. Quantization error generated by this rounding process can be canceled in the digital domain [7]. The feedback DAC is implemented with voltage-mode analog switches for the *RC* integrator, and current switches for the *gm-C* integrator. A circuit schematic of the *gm-C* integrator and feedback DAC is shown in Fig. 6.

The counter causes a missing operation because of the meta-stable state of the flip-flop, where a single pulse is counted as double or as nothing. Because this count error degrades SNR, the relationship between the SNR and the counter error rate was investigated with a functional simulation at several specified error rates. To prevent the count error, a gray code counter is effective, because a node voltage transition is always single and the count error can be simply corrected.

Furthermore, low-power digital filters for decimation and anti-aliasing are necessary to transform pulse density modulation (PDM) signals into binary digital signals. Chip layout must be designed very carefully, because the SNR is reduced by the jitter of the sampling clock, which is caused especially by the coupling noise from the digital circuits.

IV. Simulation Results

A. SNR

Functional simulations were performed considering the nonlinearity of VCO gain obtained through SPICE simulation. Spectra of output-PDM signals were calculated by decimation filtering and fast

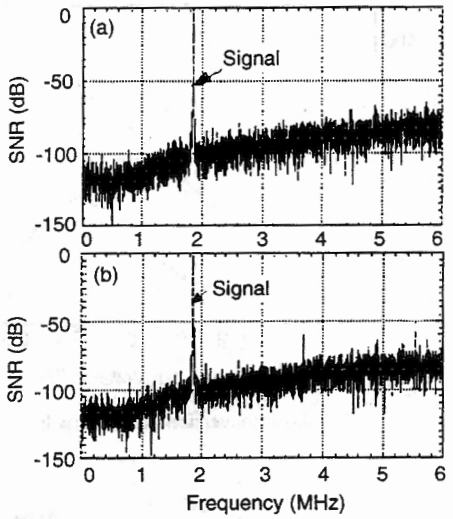

Fig. 7. Simulated spectra of VCO-DS-ADC output signals. (a) Linear VCO quantizer is assumed. (b) Nonlinearity of VCO, shown in Fig. 5, is considered.

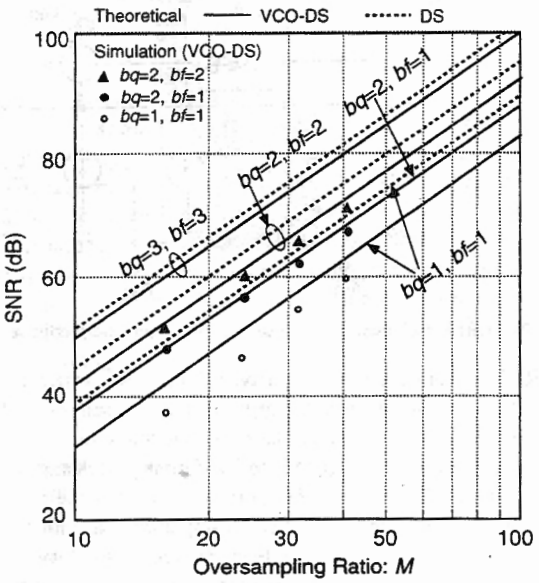

Fig. 8. SNR's of VCO-DS-ADC's. Signal bandwidth = 5 MHz, Nyquist frequency = 10 MHz, bq = bit of quantizer, and bf = bit of feedback DAC. Non-linearity of the VCO is not considered. Theoretical values are calculated by (6) and (7). Simulation is carried out by using the discrete-time functional simulator (SPW).

Fourier transform (FFT). Fig. 7(a) shows the spectrum using a linear VCO model, and 7(b) shows a VCO model with 1.3% nonlinearity, as shown in Fig. 5. The nonlinearity of the VCO causes harmonic distortions at the converter output and degrades SNR characteristics.

SNR characteristics were evaluated by the functional simulation and theoretical calculation using (6) and (7). The VCO quantizer resolution (bq) and the feedback DAC resolution (bf) were set as follows: (a) $bq = bf = 1$ bit, (b) $bq = bf = 2$ bits, (c) $bq = bf = 3$ bits, and (d) $bq = 2$ bits and $bf = 1$ bit. The simulated SNR's and theoretical SNR's are shown in Fig. 8. As shown in the figure, the theoretical SNR characteristics of VCO-DS-ADC are lower than those of the conventional DS-ADC, because the input range of VCO is limited to $(2^{bq} - 1)/2^{bq}$. Furthermore, the simulated SNR degrades by 3 dB over the theoretical value for 1-bit quantization. The degradation decreases to less than 1 dB for 2-bit quantization. From these simulated SNR's, a VCO-DS-ADC with a 5-MHz bandwidth

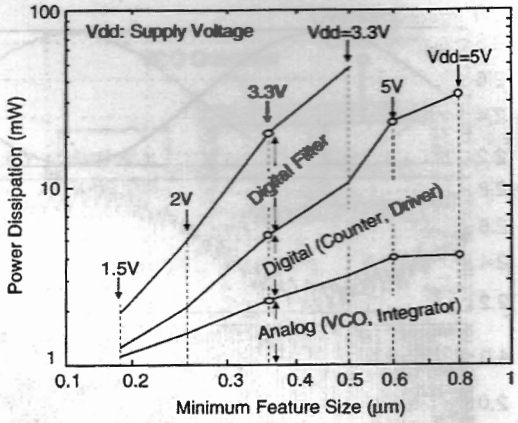

Fig. 9. Estimated relation between power dissipation and minimum feature size of CMOS technologies.

and a 59-dB SNR is attained with 1-bit quantizer and an oversampling ratio (M) of 40. If 2-bit quantization and 2-bit feedback are used, a 69-dB SNR is obtained at $M = 40$, and a 59-dB SNR is obtained with $M = 24$. If 2-bit quantization and 1-bit feedback are used, a 59-dB SNR is attained at $M = 28$.

B. Power Dissipation

Fig. 9 shows the estimated relation between the dissipation power and minimum feature size of CMOS technologies. In the figure, white circles indicate simulation values for 0.35-, 0.6-, and 0.8-μm CMOS technologies. Power dissipation of the ADC was lower than that found in other methods. For example, a converter with a 5-MHz bandwidth and 400-MHz oversampling was designed with 5-mW power dissipation utilizing a 0.35-μm CMOS and a 3.3-V supply voltage. The proposed ADC will become more effective, if implemented with deep sub-μm CMOS technologies and operated at a low supply voltage, because almost all circuits are digital, and accurate analog circuits such as operational amplifiers are not required. The VCO power dissipation will be reduced in proportion to the supply voltage: V_{dd}, and those for logic parts will be reduced in proportion to V_{dd}^2. Based on this V_{dd} dependence, the estimated power dissipation will decrease to as low as 2 mW for a 0.18-μm CMOS and a 1.5-V supply.

V. Conclusion

We propose the architecture of an oversampling delta–sigma ADC utilizing the VCO as a multibit quantizer. The architecture realize a 59-dB SNR and a 5-MHz wideband with 1-bit quantization. If the multibit VCO quantizer is used, an SNR or bandwidth can be improved. The proposed VCO-DS-ADC will find new application areas for oversampling ADC's, and bring a smart embedded converter into deep sub-μm mixed-signal CMOS VLSI's.

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References

[1] J. Candy and G. Temes, Eds., *Oversampling Delta-Sigma Data Converters*. Piscataway, NJ: IEEE, 1992.

[2] M. Erber, H. Schemmann, and M. Rieger, "Second order delta-sigma modulator for video signal processing," in *Proc. IEEE Int. Conf. Consumer Electronics' 96*, WPM 5.7, 1996.

[3] T. Brooks, D. Robertson, D. Kelly, A. Muro, and S. Harston, "16 bit delta-sigma pipeline ADC with 2.5 MHz output data-rate," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 1997, pp. 208–209.
[4] K. Uchimura, T. Hayashi, T. Kimura, and A. Iwata, "Oversampling A-to-D and D-to-A converters with multi-stage noise shaping modulators," *IEEE Trans. Acoust., Speech, Signal Processing*, vol. 36, pp. 1899–1905, Dec. 1988.
[5] A. Iwata and M. Nagata, "A concept of analog-digital merged circuit architecture for future VLSI's," *IEICE Trans. Fundamentals Electron., Commun., Comput. Sci.*, vol. E79-A, no. 2, pp. 145–157, 1996.
[6] M. Nagata, J. Funakoshi, and A. Iwata, "A PWM signal processing core circuit based on a switched current integration technique," *IEEE J. Solid-State Circuits*, vol. 33, pp. 53–59, 1998.
[7] T. Leslie and B. Singh, "An improved sigma-delta modulator architecture," in *Proc. IEEE ISCAS '90*, pp. 372–375.