Low Power 1 GHz Frequency Synthesizer LSI's

YUKIO AKAZAWA, HIROYUKI KIKUCHI, ATSUSHI IWATA, TAKASHI MATSUURA, AND TORU TAKAHASHI

Abstract—To realize a low-power low-cost highly-reliable frequency synthesizer for a 1 GHz band radio, a bipolar prescaler IC, and a CMOS LSI, consisting of a programmable counter, phase frequency comparator, and fixed divider, have been developed. The PLL synthesizer principle, using a pulse swallow counter, has been adopted for 1 GHz direct programmable count down. Adopting an advanced bipolar process and a diode AND circuit for the dual modulus prescaler IC, high frequency operation at 1 GHz and 150 mW low power dissipation have been achieved simultaneously. To reduce the loop delay in the CMOS programmable counter, which limits the operating frequency, a new circuit configuration for the programmable counter and pulse swallow counter is adopted.

As a result, 1 GHz frequency synthesizer LSI's have been developed with 150 mW low power dissipation for the prescaler IC and 18 mW low power dissipation for CMOS LSI.

I. Introduction

FOR a number of years, frequency synthesizers have been used in many kinds of communication systems. They have been made based on conventional analog circuit technology, mixing, and filtering techniques. Because these techniques needed fine adjustments and/or highly precise components, synthesizers were expensive. Furthermore, power saving and physical dimensions are strongly required, especially for mobile radio systems.

Since LSI technology has advanced year after year, the phase locked loop (PLL) synthesizer technique has become effective in solving the above problems [1]-[3]. The PLL synthesizer consists of a voltage controlled oscillator (VCO), programmable frequency divider (PFD), loop filter (LF), phase frequency comparator (PFC), and a reference oscillator. Digital circuits, such as PFD and PFC, are suitable for LSI technology, which enables a reduction in their cost. VCO and LF are high-speed analog circuits, so they are difficult to realize in a monolithic IC. A major difficulty in integration of the PFD and PD circuits is to simultaneously satisfy two inconsistent requirements, the very high frequency operation and a low power dissipation. To satisfy both the requirements at the same time, two LSI's have been developed. One is a dual modulus bipolar prescaler IC that makes it possible to divide up to 1 GHz, and the other is a CMOS LSI for the PFD, PFC, and fixed divider that operates with low power. Furthermore, as much refinement as possible was made in designing circuit configurations for reduction in power dissipation and to assure high frequency operation.

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This paper describes design and performance data for these LSI's.

II. Frequency Synthesizer Configuration and Performance Objectives

Basically, a PLL synthesizer consists of VCO, PFD, PFC, and LF. The PFD is most suitable for LSI technology, because it can be composed of an all digital circuit and requires a large number of components. However, it is very difficult to realize high frequency operation with low power dissipation using LSI technology. To realize a radio frequency snythesizer, therefore, several PLL synthesizer configurations, namely, a heterodyne method, a fixed prescaler method, and a pulse swallow method, have been developed.

The pulse swallow category, using a pulse swallow counter, can be composed of low-speed digital circuits, except for a slightly high-speed part, prescaler, and does not degrade any loop characteristics, such as loop gain and channel switching time, so that it is the most profitable for LSI realization.

On the contrary, a heterodyne method, employing the heterodyne principle, has a disadvantage in that a mixer and a tuned filter, not compatible with LSI technology, are needed. A fixed prescaler method, formed by inserting a fixed divider in front of a low-speed PFD, is not suitable either. Insertion of the fixed divider, whose divide value is F, reduces the PFC operating frequency to $1/F$, comparing the direct programmable counter method. In this case, loop bandwidth becomes narrow and LF design becomes difficult.

As shown in Fig. 1, the pulse swallow synthesizer circuit configuration consists of a dual modulus prescaler, $\div A$ counter and $\div M$ counter. Synthesized output frequency f_o is given by

$$f_o = (M \times P + A) \times f_{ch} \tag{1}$$

where M, P, and A are divide values for $\div M$ counter, dual modulus prescaler and $\div A$ counter, and f_{ch} is the channel spacing frequency, respectively. The dual modulus prescaler divide value is obviously P or $P+1$. The prescaler was designed to achieve 1 GHz maximum operating frequency in order for it to be successfully applied to many kinds of radio systems. The $\div A$ and $\div M$ counters need no high frequency operation, unlike the prescaler; they need only $1/P$ GHz. For low power dissipation, therefore, the prescaler has been formed with bipolar technology and $\div A$ and $\div M$ counters have been integrated with the PFC and fixed divider on a single chip utilizing CMOS technology.

The smaller the prescaler divide value, the lower the power dissipation, and the more high frequency operation CMOS LSI needs. Therefore, considering the production level CMOS technology ability, 128 was selected as divide value P. Divide

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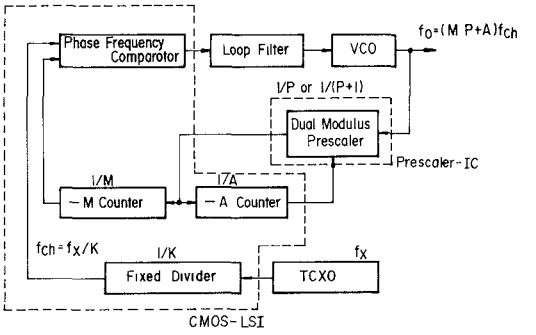

Fig. 1. Synthesizer configuration using pulse swallow counter.

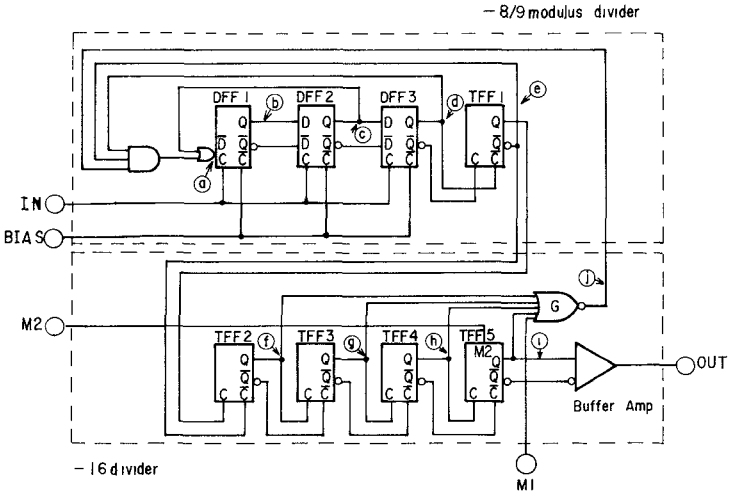

Fig. 2. Dual modulus prescaler IC block diagram.

values M and A depend on P, f_{ch}, and the maximum input frequency for the PFD, f_{max}. When f_{max} and f_{ch} are 1 GHz and 25 kHz, respectively, the total divide value for the synthesizer is 40 000. Divide values for $\div A$ and $\div M$ counters need to be in the 0 to 127 range and in the 128 to 511 range, respectively. In detail, therefore, the total divide values are in the 16 385 to 65 535 range; that covers the frequency band for many kinds of radio systems.

III. Dual Modulus Prescaler IC

A. Circuit Operation Outline [4]

A dual modulus prescaler block diagram is shown in Fig. 2. The $\div$ 8/9 dual modulus divider, which consists of an AND gate, OR gate, and 4 flip-flops, counts down to an 8/9 modulus. The latter stage, which consists of a ripple counter with 4 flip-flops, divides the output of the previous stage to 1/16. In the case of $\div$ 128, the 8/9 divider counts 8 constantly. On the other hand, at the $\div$ 129 operation, it counts 8 or 9 according to the G gate output, that is the NOR gate with 5 inputs. When the latter count is 16, the G gate output is high. After another 15 durations, it is low. Therefore, if the $\div$ 8/9 divider is designed so as to count 9 at high G gate output, the 129 count value can be obtained. Fig. 3(a) shows a timing chart for the prescaler. A synchronous shift counter was adopted to the $\div$ 8/9 dual modulus divider for high speed and stable operation. The second D flip-flop output is fed back to the first stage through the OR gate to perform a 4-count operation. The third D flip-flop performs shift operation and the fourth T flip-flop counts 2. Therefore, these 4 flip-flops count 8 totally. The $\div$ 9 operation is realized by feeding back the third and fourth flip-flop outputs to the first stage through an AND gate and an OR gate. When this feedback path is available, first and second D flip-flops operate as a $\div$ 5 divider. Therefore, total divide value is 9. Fig. 3(b) shows a timing chart for $\div$ 9 and $\div$ 8 operations.

Additional functions were designed, such as the reset function for prescaler function test ease and $\div$ 64/65 dual modulus operation for many applications.

B. Circuit Design

The maximum prescaler operating frequency is limited by the delay in the feedback path from the third D flip-flop to the first flip-flop through an AND gate and OR gate at the $\div$ 9 operation for the $\div$ 8/9 divider. Considering more details about this limitation, it is critical when the AND gate output transits from 1 to 0 by the 10th clock input shown in Fig. 3(b). It is assumed that the D flip-flop is the master-slave flip-flop, which reads data at a clock rising edge and outputs at a falling edge. Since clock duty is 50 percent, this AND operation must perform up to the next 11th clock rise, as is shown in Fig. 3(b). Therefore, the maximum input frequency is expressed by

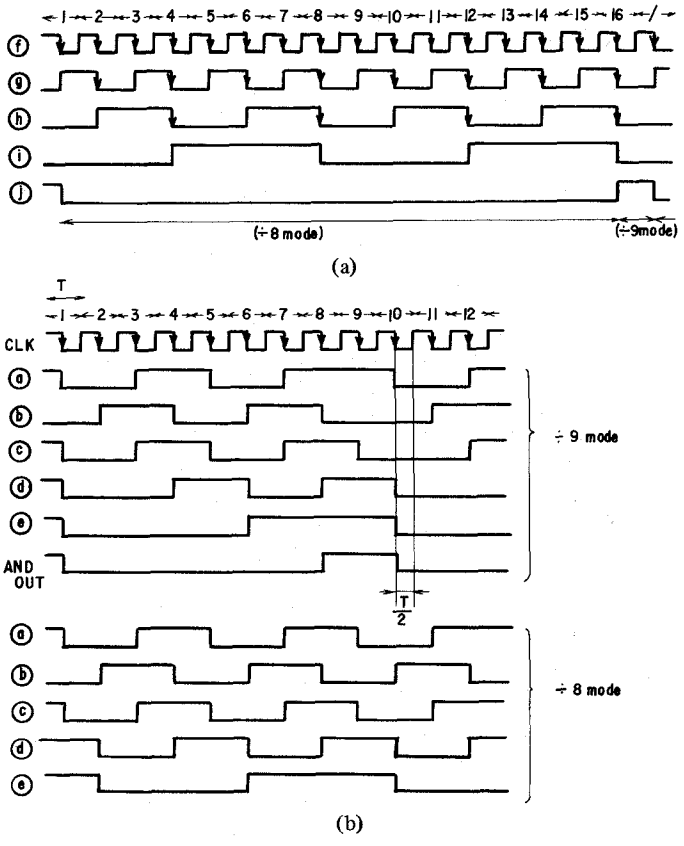

Fig. 3. Timing chart for dual modulus prescaler. (a) Latter stage. (b) ÷ 8/9 divider stage.

$$f_{\max} = \frac{1}{2 \times (T_{DF/F} + T_{\text{AND}} + T_{\text{OR}})} \tag{2}$$

where $T_{DF/F}$ is the D flip-flop delay time from the clock falling edge when the third D flip-flop transits from 1 to 0, T_{AND} is the AND gate delay time, and T_{OR} is the OR gate delay time. The OR gate can consist of a current mode logic circuit with a small delay time, usually so that its delay time is negligible. Therefore, the delay time reduction in the AND gate and D flip-flop is the key point for improving maximum operating frequency. Fig. 4 shows the AND gate and first stage D flip-flop circuit configuration. The D flip-flop is an LCML (low power current mode logic) master-slave flip-flop and all other flip-flops have the same configuration. The diode AND circuit was adopted, as shown in the part enclosed by a broken line in Fig. 4.

As previously described, it is desirable that the transition from 1 to 0 be as fast as possible. This requirement is satisfied by using an AND diode. Furthermore, this circuit is simpler, occupies smaller chip area, and dissipates less power than other circuits.

C. Chip Realization and Performance

To achieve both high speed and low power dissipation at the same time, it is important to improve the device characteristics. Advanced bipolar processes have been developed, which adopt a shallow junction, dielectric isolation, walled emitter, and self-alignment techniques. The device parameters are

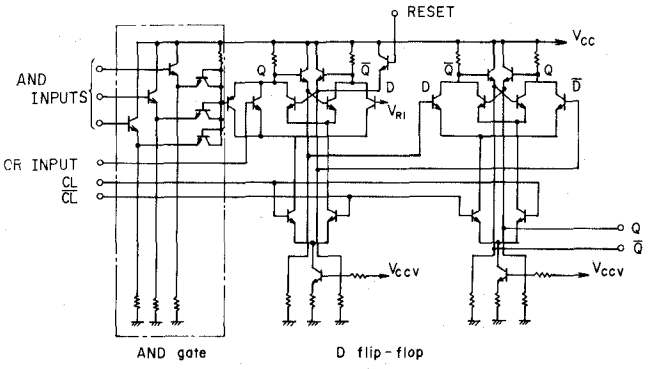

Fig. 4. AND gate and D flip-flop circuit configuration.

TABLE I
BIPOLAR DEVICE PARAMETERS

(Emittersize; $4 \times 2 \mu m^2$)

Parameters	Values
f_T	4 [GHz]
C_{JE}	0.039 [pF]
C_{JC}	0.036 [pF]
C_{CS}	0.126 [pF]
R_B	393 [Ω]
R_C	180 [Ω]
R_E	4 [Ω]

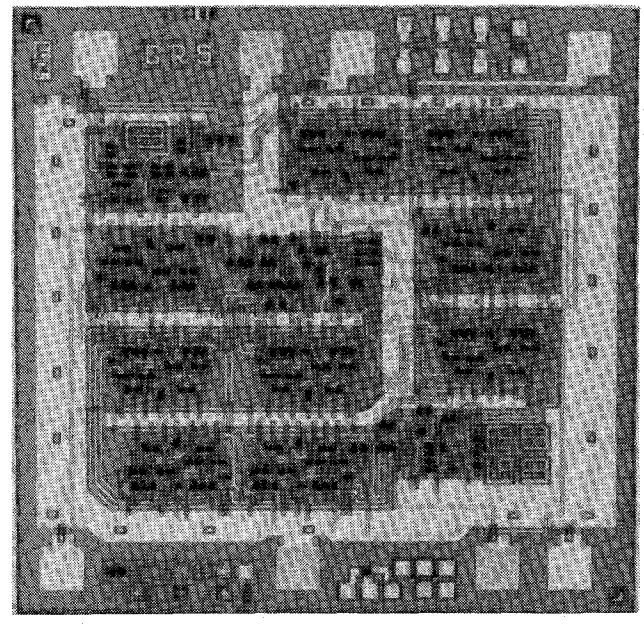

Fig. 5. Dual modulus prescaler IC chip photograph.

shown in Table I. The f_T and base resistance are improved simultaneously. The switching speed for the basic LCML circuit is 0.3 ns/gate at 1 mA/gate, which is estimated by circuit simulation. The maximum operating frequency for the prescaler estimated by circuit simulation was 1.25 GHz at 400 $mV_{p\text{-}p}$ input signal level and 5 V supply voltage.

A chip photograph appears in Fig. 5. Chip size is 1.56 × 1.59 mm, including about 200 transistors, 140 resistors, and one 10 pF capacitor. This chip is packaged in a small 8-pin

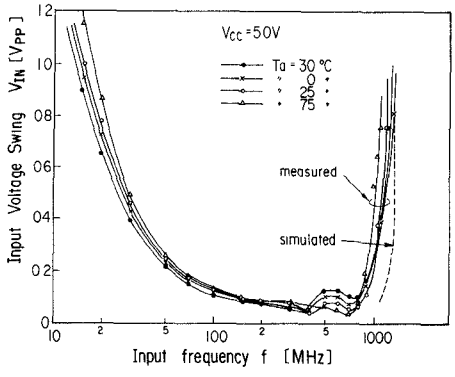

Fig. 6. Dual modulus prescaler IC measuring characterisitcs.

TABLE II
DUAL MODULUS PRESCALER IC PERFORMANCES

Items	Spec values
Divide values	128/129 or 64/65 dual modulus
Maximun operating frequency	~1.08 GHz
Supply voltage	5 V (±5%)
Drawing current	30 mA Typ
Ambient temperature range	-30 ~ 75 °C
Input signal level	400~1200 mV_{PP}
Output signal level	1.2 V_{PP} Typ
Output rising time	20 ns MAX (C_L=10pF)
Divide mode switching settingup time	20 ns MAX
Package	8 pin plastic mold DIP

plastic mold DIP in order to reduce equipment size and production cost.

Fig. 6 shows measured frequency characteristics for minimum input voltage swing, that result in correct operation. In other words, correct count down operations are observed in the upper area of the characteristics curves. The maximum operating frequency is about 1.08 GHz under typical conditions, which nearly agrees with the simulated value shown in the broken line. Even if the IC is used under the worst-case conditions with 50°C temperature deviation, correct operation is maintained up to 950 MHz at a 400 mV input voltage swing. Power dissipation is as small as 150 mW at a 5 V supply voltage. Table II shows dual modulus prescaler performances.

IV. CMOS LSI

PFD, PFC, FD, and shift register (SR), for setting up the divide value by serial data, were integrated on a single chip utilizing CMOS process technology. Fig. 7 shows a CMOS LSI block diagram.

A. Circuit Descriptions and Designs

Programmable Frequency Divider: The $\div A$ and $\div M$ counters were composed of 4-bit binary programmable counters (4 bit BPC) in order to obtain ease in setting up the divide value by binary data and applicability to any kind of radio equipment. The $\div A$ counter needs two 4 bit BPC's and the $\div M$ counter needs three to get the required divide value, as mentioned previously. The 4 bit BPC consists of the D flip-flops and has functions programming the count values P_n by the LOAD

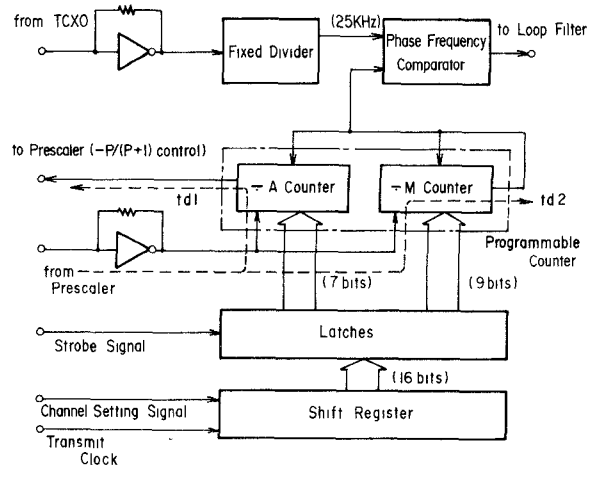

Fig. 7. CMOS LSI block diagram.

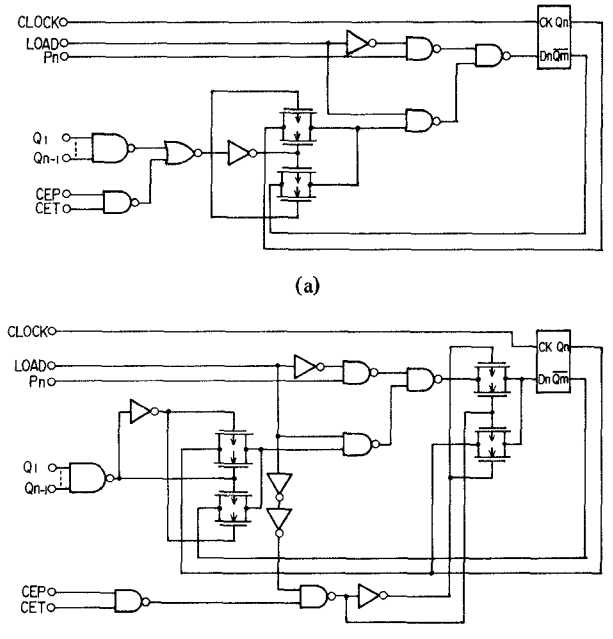

Fig. 8. Programmable counter (nth bit). (a) Original circuit. (b) Improved circuit.

signal, activating the counter operation by the CEP signal, and activating the operation and output by the CET signal. These functions are expressed by the following logic equations:

$$D_n = \overline{\text{LOAD}} \cdot P_n + \text{LOAD} \cdot (((\overline{\text{CEP} \cdot \text{CET}}) \cdot (\overline{Q_{n-1} \cdots Q_1})) \cdot Q_n + ((\text{CEP} \cdot \text{CET}) \cdot (Q_{n-1} \cdots Q_1)) \cdot \overline{Q_n})$$

$$= \overline{\text{LOAD}} \cdot P_n \cdot \text{LOAD} \cdot ((\text{CEP} \cdot \text{CET}) + (\overline{Q_{n-1} \cdots Q_1})) * Q_n \quad (3)$$

where D_n represents data input for the nth bit D flip-flop and * represents Exclusive-OR. Fig. 8(a) shows the circuit configuration for (3). The number of circuit elements and the delay time were reduced by realizing the Exclusive-OR using CMOS transmission gates. The CMOS programmable counter

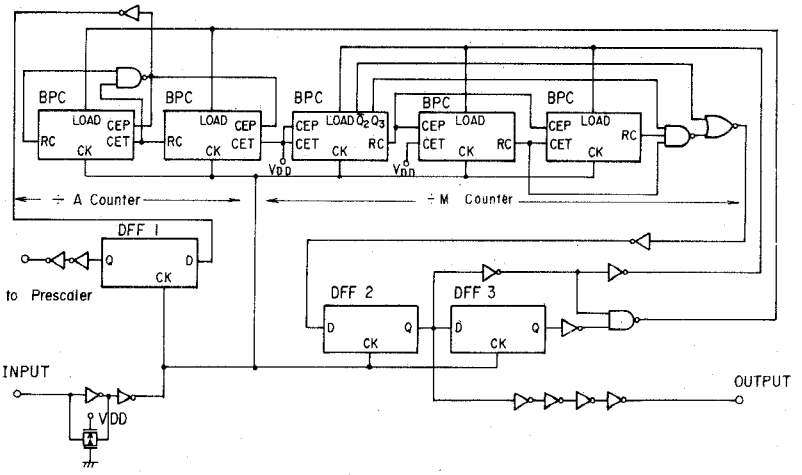

Fig. 9. PFD block diagram.

performance was examined by circuit simulation and preliminary fabrication. As a result, there was a little margin in the operation frequency. Loop delay values t_{d1} and t_{d2}, shown in Fig. 7, were especially large. To reduce these delays, two new circuit techniques have been adopted.

The first technique is related to the 4 bit BPC and is as follows. The critical path for the 4 bit BPC is the path from the CEP or the CET signal input to the *D* input. Therefore, CMOS transmission gates were as inserted in front of the *D* flip-flop. These gates enable the start/stop control operation time to be reduced by the delay time in two NAND gates with two inputs. Nevertheless, when the 4 bit BPC starts to count, the hazard arises in the signal which controls the transmission gates inserted in front of the *D* flip-flop because the LOAD signal arrives earlier than the CEP and CET. This hazard causes a delay in the count start operation. Therefore, two inverters were added on the path from the LOAD signal terminal, as shown in Fig. 8(b), so as to make the LOAD signal arrive later than the CEP and CET.

The second techinque is related to overall pulse swallow counter configuration and is as follows. In conventional circuit configurations, loop delay time t_{d1} is equal to the sum of $\div A$ counter delay time t_a and t_{ps}, that is, delay time for the prescaler when changing the prescaler divide value. As the prescaler divide value may be changed at any clock period of the $\div M$ counter operation, the *D* flip-flop (*DFF*1) can be inserted in back of the $\div A$ counter to separate the critical path, as shown in Fig. 9. This insertion makes t_{d1} small. In other words, t_{d1} is the larger of t_a and t_{PS}. Loop delay t_{d2} for LOAD set up operation can be reduced similarly, using the *D* flip-flop (*DFF*2 and *DFF*3).

The level converter which converts the output voltage swing from the prescaler, 1.2 $V_{p\text{-}p}$, to the CMOS level, 0 to 5 V, was integrated using an inverter with high resistance feedback. Its chip area was reduced by forming the feedback circuit with p- and n-channel MOS transistors, which are biased at a conductive state all the time, instead of a resistor.

Phase Frequency Comparator [5]: The PFC, detecting the phase difference between the reference signal and the PFD output, consists of flip-flops with a set-reset function. The charge pump circuit is a tri-state output CMOS gate, consisting of p-channel and n-channel transistors. The charge pump converts the phase difference into the amount of the charge. It is also integrated into the same chip. In order to reduce the dead zone for the PFC, which causes phase jitter, critical path delay time for PFC was minimized.

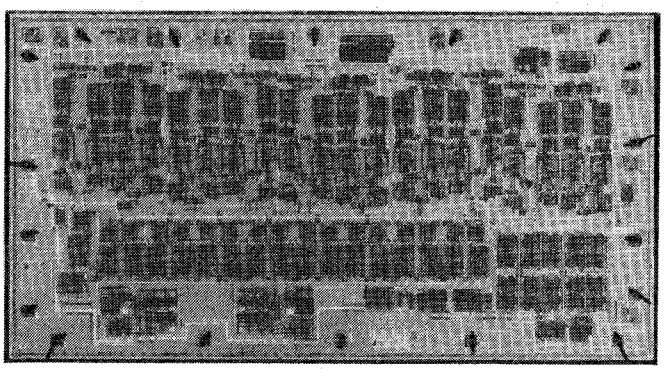

Fig. 10. CMOS LSI photograph.

The noise in the PFC, the charge pump, and the loop filter does not affect the synthesizer characteristic. Because its noise is caused mainly by the VCO, it can be realized with pure spectrum characteristics by a SAW resonator and a hybrid IC technology.

Fixed Divider: The reference signal, supplied from the TCXO (temperature compensated crystal oscillator), is divided by this divider, to get the PFC reference input, namely, channel spacing frequency. As it is easy to realize TCXO frequency range from 10 MHz to 20 MHz, the maximum frequency was designed to be larger than 20 MHz using the static CMOS binary counter with CMOS transmission gates.

B. Chip Realization and Performance

A chip photograph appears in Fig. 10. It was fabricated using a 3.5 μm silicon-gate CMOS process. Chip size is 2.95 X 5.62 mm, including about 2200 MOS devices. This chip is packaged in an 18 pin DIP.

The fixed divider maximum input frequency dependence on temperature is shown in Fig. 11. The PFD maximum input frequency dependence on temperature is also shown in Fig. 11. Maximum frequency deviations between samples are within

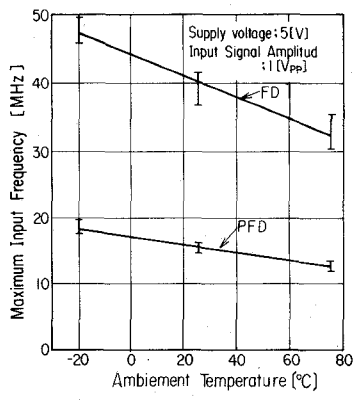

Fig. 11. Measured maximum input frequency for CMOS, PFD, and FD.

TABLE III
CMOS LSI PERFORMANCES

Circuits	Items	Values
Phase frequency comparator	Channel switching time	< 70 ms
Fixed divider	Divide value	512 (1024)
	Maximum operating Frequency	38MHz (Typ. Conditions)* 27.6MHz (V_{DD}=4.5V, Ta=75°C, Imput level=1.0V_{PP})
	Power dissipation	5mW (V_{DD}=5V, Input signal: 1 V_{PP}, 12.8 MHz)
Programmable divider	Divide Value (including Prescaler IC operation)	16383~65535
	Maximum operating Frequency	15.5 MHz (Typ. Conditions) 10 MHz (V_{DD}=4.5V, Ta=75°C, V_{IN}=1.0V_{PP})
	Power dissipation	13mW (Typ. Conditions)
Shift Resister	With Serial in - Parallel out function	

* Typ. Condition ; V_{DD}=5V, Input signal level=1.0V_{PP}, Ta = 25°C

±10 percent for the fixed divider and within ±5 percent for the PFD, as shown in Fig. 11. Power dissipation is typically 18 mW at a 5 V supply. Table III summarizes CMOS LSI performance.

An experimental 800 MHz band synthesizer has been made using these LSI's. Superior synthesizer performance has been achieved as follows. Channel switching time is about 70 ms. *C/N* (ratio carrier-to-noise) is larger than 77 dB and reference leak is 90 dB [6].

V. SUMMARY

To realize a low power and small PLL synthesizer, a dual modulus prescaler IC, and CMOS LSI for a 1 GHz PLL synthesizer have been developed based on the pulse swallow principle. By adopting an advanced high-speed bipolar process and a diode AND circuit for the prescaler IC, high frequency operation, up to 1 GHz, and 150 mW low power dissipation have been simultaneously achieved.

A programmable frequency divider (PFD), fixed divider (FD), and phase frequency comparator (PFC) have been integrated into the CMOS LSI. To reduce loop delay limiting operation frequencies, circuit configurations for the programmable frequency divider and pulse swall counter have been improved. A 16 MHz PFD operation and 40 MHz FD operation have been obtained with 13 mW and 5 mW power dissipation, respectively. As a result, low power and the 1GHz PLL frequency synthesizer have been realized with the 2 chip set.

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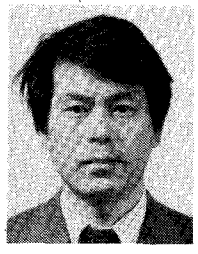

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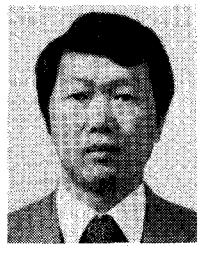

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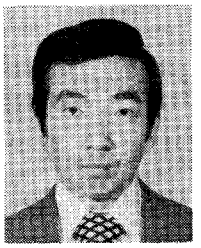

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Low-Power High-Drive CMOS Operational Amplifiers

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Abstracts—**Low-power CMOS op amps with high-drive capability and good settling characteristics are described. One circuit, occupying 150 mils^2 of active area and consuming 1 mW of power drives a capacitive load of up to 150 pF with greater than ±2.5 V/μs slew rates and less than 3.5 μs settling time to 0.1 percent. A somewhat larger circuit drives low-resistance (e.g., 600 Ω) and high-capacitance (1000 pF) loads with better slew rates and settling time. These circuits are suitable for applications in such systems as charge-redistribution codecs and switched-capacitor filters.**

I. Introduction

THIS paper describes CMOS operational amplifier circuits, suitable for switched-capacitor filter and charge-distribution network applications, which feature a small chip area and low power dissipation (relative to previous designs) while achieving excellent small-signal and large-signal performance. Operating from ±5 V supplies, the amplifiers typically have 80 dB of gain over a ±3 V output range, 60 degree phase margin, 1-8 MHz of bandwidth depending on loading and processing variations, better than 3.5 μs settling time to 0.1 percent, and 30 nV/$\sqrt{\text{Hz}}$ of broad-band noise at the input, with a noise bandwidth only 10 percent greater than the signal bandwidth.

Two circuits are described. The first is a two-stage design dissipating 1 mW and occupying 150 mils^2, with slew rates greater than ±2.5 V/μs. It contains a network that brings a biasing transistor of the common-source output stage into play as a signal amplifying device at high frequencies and during load-limited slewing. This circuit has been used throughout a charge redistribution codec having switched capacitor filters [1]. The second circuit is a three-stage design capable of driving a 600 Ω load (or a capacitance up to 1000 pF) with ±10 V/μs slew rates and 2 μs settling time; it contains a dual-path middle stage. This design, which has not yet been implemented in its final form, is the outgrowth of work on a similar circuit that was fabricated. The changes made, supported by extensive computer simulations, improve the phase margin and extend the range of good linearity. Actual performance results are presented for the two-stage design; results of computer simulations are given for a three-stage design.

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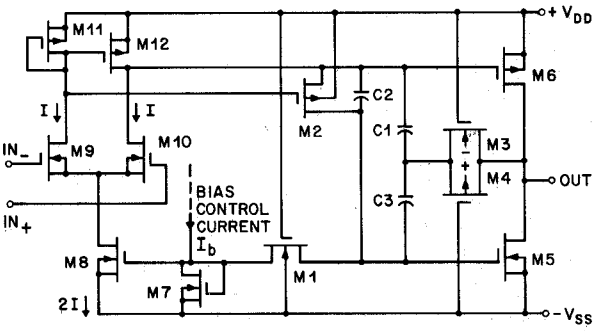

Fig. 1. Fast-settling low-power CMOS op amp.

II. Circuit Descriptions

A. Two-Stage Op Amp

The basic form of the first op amp, a two-stage design for driving low-conductance loads, is shown in Fig. 1. Without the elements $M1$ (replaced by a short circuit), $M2$, $C2$, and $C3$ (removed), and with the main shaping element $C1$ connected as a Miller capacitor directly to the output ($M3$ and $M4$ shorted out), the circuit would be considered conventional [2], [3].

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