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Optical Interconnections as a New LSI Technology

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SUMMARY This paper was written for LSI engineers in order to demonstrate the effect of optical interconnections in LSIs to improve both the speed and power performances of 0.5 and 0.2 μm CMOS microprocessors. The feasibilities and problems regarding new micronsize optoelectronic devices as well as associated electronics are discussed. Actual circuit structures clocks and bus lines used for optical interconnection are discussed. Newly designed optical interconnections and the speed power performances are compared with those of the original electrical interconnection systems.

key words: *optical interconnection, CMOS micro processor, laser diodes, photo ditectors, optical wave guides, multichip module, clock circuit, bus line*

1. Introduction

This article was written for those working in the field of LSIs. Optical interconnection is a technology which will be necessary to overcome the communication crisis concerning ultra-scale LSIs in the next decade. The characteristics of light are complementary to those of electron. Difficulties concerning electronic signal interconnections, delay, couplings and noise, which stem from the inherent characteristic of the electron will be removed by the use of light, photons, which have completely different physical nature characteristics from those of electrons. It is rather natural to use electrons as carriers for logical operation and photons as carriers for information transfer, "the optical interconnection".[1]

People have already started to use optical interconnections inside of computers between boards. This trend will proceed to more extensive use inside of computers, between chips and, finally, inside LSIs.[2]

This paper presents a model circuit analysis in order to illustrate various problems concerning signal delay and power dissipation in large-scale CMOS microprocessors and compares with the same systems which utilize optical interconnections. Improved performance concerning both delay and power dissipation is illustrated by using optical interconnection.

Section 2 presents an estimate of electrical wiring delay in LSI chips and compared with that of optical interconnections. Delays and power analysis were studied in 0.5 and 0.2 μm CMOS micro processors and compared with a new version in which optical interconnections are applied to clocks and bus lines.

Section 3 considers the intrinsic characteristics of optical interconnections as well as the feasibilities on micronsize lasers, detectors and optical waveguide systems. The feasibilities of fabrication technologies are also discussed.

Section 4 looks at the importance of the LSI interconnection technologies for future electronics as well as optical systems. In such technologies collaboration between people in related fields is essential.

2. Optical Interconnections in Advanced CMOS Microprocessors. A Quantitative Analysis Concerning Speed and Power Performance

2. 1 Problems Concerning Electrical Interconnections in LSIs

As the minimum feature size of transistors has been scaled down, the delay time and chip area of basic logic gates, or flip-flops, have been drastically reduced. However, interconnection technologies are still a major concern in high-performance LSIs, since the capacitance and resistance of on-chip wires increase rapidly as the chip size is increased and the minimum feature size is decreased. Thus, high-speed, high-density interconnections are vital for high-performance LSIs.

The speed of a digital LSI is determined by the delay times of the logic circuits and the interconnection wiring. If the wire length is of the same order as the chip size, the delay time due to wiring is dominant, compared with the gate delay time for a no-wiring load. In a typical application-specific integrated circuit (ASIC), about 80% of the wires are shorter than 1 mm, since they are used for local interconnections, however about 1% of the wires used for global interconnections are as long as the die size.

As the gate complexity increases, the interconnection density limits the integration scale in ULSIs, because the wiring occupies more than 80% of the chip area. The ratio of the wiring area to the gate cell area

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strongly depends on the number of interconnection layers. In the "Sea of Gates (SOG)", which is a typical ASIC, if the interconnection layer is double, only 50% of the raw gates on a master chip are usable. In triple layer interconnections, however, about 70% of the raw gates can be used. Therefore, multi-layer interconnection technologies are essential in order to integrate larger scale logic on chips.

As the minimum feature size has been reduced, an optimum scaling rule for electrical wiring has been developed regarding the line-width, line-space, metal thickness, and insulator thickness. Moreover, new conducting materials with scaled-down resistivity and new insulating materials with scaled-down dielectric constant have been studied.[3] These scaling technologies will become even more and more important in the coming quarter micron LSI era.

Another important aspect of interconnections is reliability. As the wire line-width and thickness are scaled down, the current density increases according to the square of the scaling factor. Therefore, open-circuit failures due to electro-migration have become the most severe problem. A stress-migration problem may also be solved by developing a multi-layered metal, such as Titanium/Aluminum/Titanium, and a low-stress insulator.

2. 2 Modeling and Delay-Time Estimation of Interconnections of Electrical Interconnections and a Comparison with Optical Interconnections in Global Lines

Electrical signals are transmitted from a driver gate to destination gates by charging up or discharging a wire capacitance. Therefore, this charging and discharging causes an inherent delay. If the wire length is relatively short and its resistance is lower than the impedance of the driver gate, the wiring can be characterized by a lumped capacitor. Figure 1 shows the relationship between wire capacitance and design rules, where we assume that the line-width and line-space are equal to the feature sizes described by the design rule, and the thickness as of metal and insulator are 0.5 μm and 1 μm, respectively. If the design rule is larger than 1 μm, then the wire to substrate capacitance, which is calculated by the parallel plate approximation, is dominant. Since it decreases with design rule reduction, the effect of scaling down is obvious. However, if the design rule becomes smaller than 1 μm, the wire to wire capacitance becomes dominant and it increases as scaling down continues. As is obvious from Fig. 1, the typical capacitance per unit length is 0.3 pF/mm for a 0.5 μm design rule.

If the wiring is long, its resistance is certainly not negligible, and we must therefore consider the electrical interconnections as a distributed RC line. The wire length for global interconnections becomes longer as the chip size increases. For example, the longest wire exceeds 20 mm in a 15 mm square SOG chip designed with a conventional CAD tool. Figure 2 shows the delay time versus wire length calculated with a distributed RC line model. It shows that the delay time of a 20 mm long wiring with a 0.5 μm design rule is over 5 ns, and it exceeds 20 ns with a 0.2 μm design rule.

Furthermore, if the operating frequency becomes high, the reactance of the wiring becomes larger than

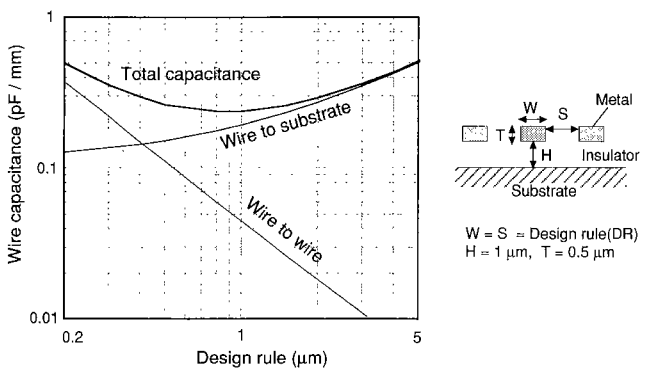


Fig. 1 Wire capacitance vs. design rule.

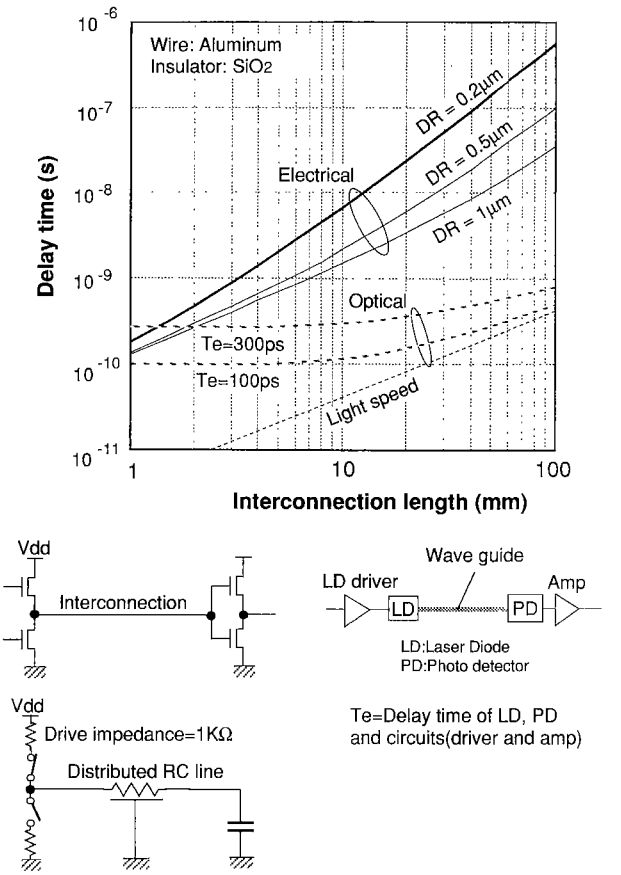


Fig. 2 Delay time of electrical and optical interconnections.

the resistance. In this case, interconnections are considered as an LC transmission line. Besides the delay time, we must evaluate cross talk and power line noise caused by electrical coupling among the wirings to maintain a large noise margin in a logic operation.

Since optical interconnections, comprising of wave-guides, light sources, and photo detectors do not charge and discharge parasitic capacitance of wiring, the delay time is not limited by the RC delay time or the ringing of an LC line.

The delay time for optical interconnection is also plotted in Fig. 2. A lowest line shows a delay of light signal itself in the wave guide, and two other lines correspond to a delay including T_e, which is the sum of the (E-O) conversion time in the laser diode (LD) and the photo detector (PD), plus delay due to associated electronic circuits. Since response time of optoelectronic devices is estimated to be short, tens of ps (Sect. 3. 1), T_e depends mainly on speed of electronic circuits. $T_e=100$ ps is a possible value in the future, and $T_e=300$ ps is a value, which can be realized by a 0.2 μm CMOS technology. Optical interconnection gives ten times improvement at 20 mm length, from nano seconds to sub nano seconds, and more significant improvement over several centimeters, which is important for wafer scale integrated circuits (WSI) or multichip modules (MCM).

There is no intrinsic coupling between optical interconnection lines and between an optical line and an electrical line. It is particularly beneficial for future higher frequency systems, because electrical couplings are proportional to the operational frequency whereas no such relation exist in optical interconnections.

2. 3 Model of Existing Digital LSIs and Systems

The current digital systems are based on three main technologies: the von Neumann architecture, synchronous binary logic, and large scale integration on a Si chip. The von Neumann computer consists of memory units, arithmetic logical units (ALUs), control units, and input/output (IO) units, which are connected by an internal bus, as shown in Fig. 3. The processing sequence is successively controlled by each program. A programmed instruction code is fetched and decoded in the control unit. Accoring to the code, clocks and control signals are generated and transferred to each unit. Then each unit carries out an operations to data transferred through the internal bus. In this way, instructions and data are sequentially transferred through a single bus. Therefore processing capability is limited by this operation. This is the well-known von Neumann bottleneck.

To improve the processing capability, parallel operation of circuits is used. There are two main parallel operation schemes, pipelining and multiprocessing. Recent micro-processors have used the

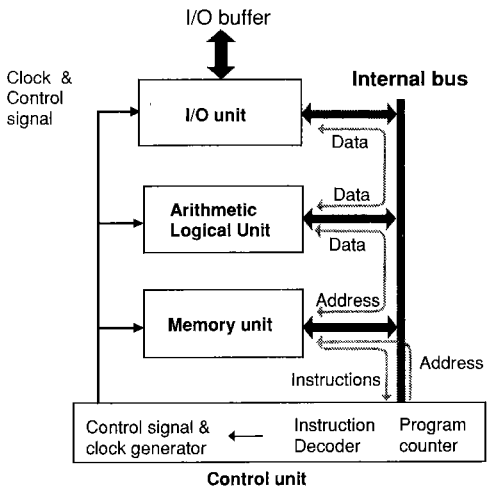


Fig. 3 Basic structure and information flow of Neumann architecture.

parallel architecture called the super-pipeline or the super-scalar. The Super Micro 2000 is one proposal for a micro processor in the 21st century.[4] This has a multi-processor architecture composed of four general purpose processors, two vector processors and one graphics processor. Its data width is 256 bits, and it uses 64 bit addressing. It will be implemented on a 25.4-mm square Si chip with 0.2-μm CMOS technology and operate at a clock frequency of 250 MHz.

Next, we discuss features of circuit technologies. Current major circuits are binary logic circuits based on Boolean arithmetic, and synchronous circuits. We can design binary logic circuits, using a combination of standard logic cells and memories, with a large noise margin. Since synchronous circuits operate by clocks, it is very important to distribute clocks with a small timing difference. This difference is called the timing skew.

A combination logic can be divided into several pipeline stages, by inserting a pipeline register in each stage. Operating each stage of the pipeline simultaneously increases the processing capability in proportion to the number of stages. The machine cycle time is given by the sum of the clock timing skew, logic delay, and setup and hold times of a register.

Use of optical interconnection in the clock circuit will practically eliminate timing skew, therefore increase machine cycle (Fig. 6). It is particularly effective at higher operating cycle time. Faster optical bus lines will be effective for communication between multi-processors.

A large scale digital system has a hierarchy of chips, modules, boards and board assembly as shown in Fig. 4. Their dimensions are 10 mm, 50 mm, 50 cm, and 1 m, respectively. If the critical path extend beyond one chip, the large capacitance of chip packaging and long interconnection cables will limit speed performance. Compact and efficient cooling methods

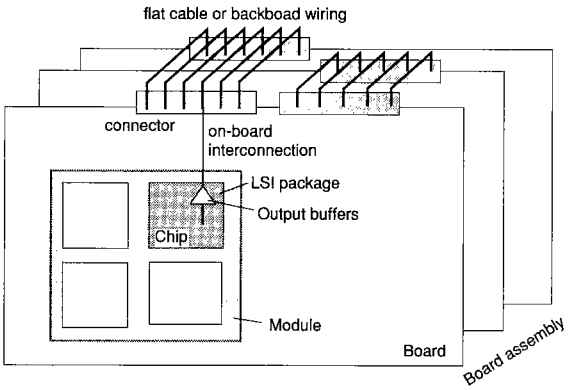


Fig. 4 Hierarchy of chip assembly.

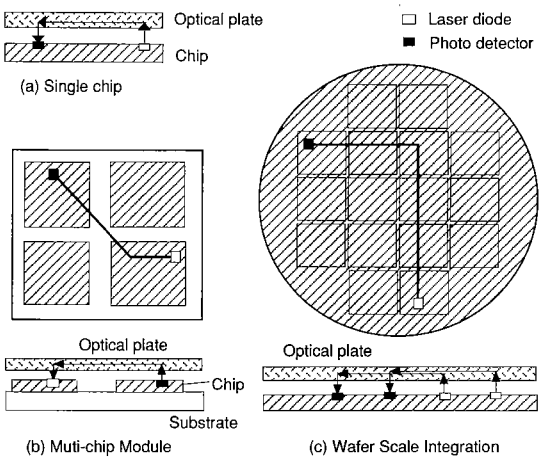


Fig. 5 Optical interconnection using optical plate.

are also important for the high performance machines such as supercomputers.

Optical interconnection has already being introduced in computers, starting from long distance interconnection. Using optical fibers, optical interconnection between boards has been used for practical application. However in these trials conventional optical techniques are used. They cannot be used for on chip optical interconnection, which is discussed in this article.

Figure 5 shows schematically feasibilities for optical interconnection in a Multi-Chip Module (MCM) and in a Wafer Scale Integration (WSI). In these structures interconnection distance extends 100 mm or more, and light signals are exchanged between spots which locate far from periphery of the chip. Therefore it is necessary to use the same optical interconnection techniques used inside of a chip. Here the new methods of optical waveguiding the "optical plate" is also used, which will be discussed more in detail (Sect. 3. 2. 3).

Impact of these optical interconnections should be enormous because of the long distances (~100 mm). As it is shown in Fig. 2, the optical interconnection delay stays at around one nanosecond at 100 mm even with the non sophisticated input output devices (large $T_e = 300$ ps). Delay of the electrical interconnection amounts a few tens of nanoseconds, even with a thick wire ($DR = 1$ μm). It is difficult to use coax type wirings in MCM, in which main part of the signal path locates inside of the chip. Whereas a structure of the optical interconnection match the requirement perfectly as indicated in Fig. 5. A strip line or a coplanar line can be used in association with a solder bump technique. However these transmission type lines creates a heating problem, because of their low impedance. Power used for optical interconnection is much smaller.

Such a short optical delay will give us not only fast operation of MCM but also large freedom of chip partitioning. In addition, the problem of crowding in the chip periphery can be relaxed by direct optical coupling at spots inside chips.

2. 4 Machine Cycle Time Calculation in Microprocessor Systems Using Either Electrical or Optical Interconnections

The machine cycle time of a binary synchronous system is determined by the sum of many delay factors as shown in Fig. 6. These factors are the gate delay with no wire load, interconnection delay due to on-chip wires, register delay, and clock timing skew. If the critical path includes data transmission through a bus, then the delay of bus line has to be added. Furthermore, if the critical path crosses several chips, two delays due to the output buffer and chip-to-chip interconnection have to be added. From the viewpoint of logic design, the delay of combination logic depends on the logic depth, that is the number of cascaded gates between registers. The logic depth can be reduced by dividing the critical path into many pipeline stages by registers. Figure 6 shows estimated machine cycle times of processors. Two architectures are compared, a single-chip CMOS processor, and a multi-chip bipolar processor. 0.5-μm and 0.2-μm design rules are considered. A micro processor with a 4-ns machine cycle time, which operates at a 250-MHz clock frequency, will be achieved using 0.2-μm CMOS, however, the speed will only be achieved at the sacrifice of power dissipation, as described in the next section.

The use of optical interconnections speeds up the processor operation in two ways, as shown in Fig. 6. First the optical clock essentially eliminates the timing skew, and only the part due to the register delay remains. Secondary, the optical bus decreases the delay. The main part of the optical bus delay is due to T_e (input and output) and bus control circuits. The total bus delay can therefore be made shorter when these electronic circuits are improved.

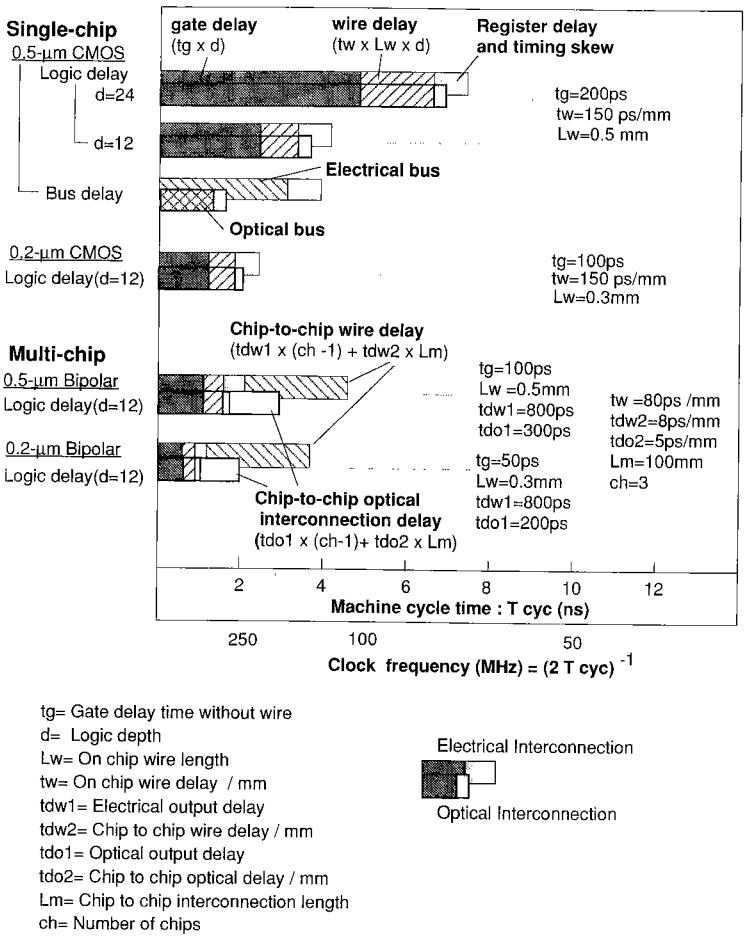


Fig. 6 Processor machine cycle time (estimated).

The optical bus will decrease the machine cycle time, when it is determined by the sum of the logic delay and the bus delay. Almost the factor two improvement can be expected in 0.5 mm CMOS (Fig. 6).

For a multi-chip bipolar, improvement of the delay utilizing optical interconnections is not very significant, since the calculation assumes that relatively small chips are interconnected by a transmission line (coplanar line), which have delays comparable with the optical type. However, the power reduction due to optical interconnection is significant. The signal power in the transmission line is several tens of mW, whereas the power required for optical interconnections should be less than one mW.

The effect of optical interconnections is significant in an MCM, as is shown in Fig. 2. The delay becomes tens of nanoseconds with electric connections. Therefore in high-speed circuits one must use transmission line in an MCM. As already pointed out, the power required for a transmission line is much larger than that of an optical interconnection, which creates problem due to heating of the entire module. In addition, one must use a flip-chip bonding technique, if a direct signal pick up from the inside of the chip is required. With this scheme however heat removal from the bonded chip will be another problem. Optical interconnections will be ideal in such application, which allow us high speed direct access and low power.

The characteristic impedance of an electronic transmission line is around 100 ohms, and is difficult to increase. However, in optical signal transmission there is no such restriction. The ratio of the input voltage to the current of a semiconductor light emitter, which corresponds to the "impedance", can be made very high. In the case of one milliwatt of laser power it is about one kΩ, and it increases by decreasing power.

For these applications, a large number of small optical devices is needed. Micron-size lasers (μ-LD) and detectors (μ-PD) are described later (Sect. 3. 2).

2. 5 Comparison on the Power Dissipation in CMOS Systems

The power dissipation in CMOS logic is determined by the charging current, leakage current, and direct-path short-circuit current. If the first term is dominant, the power dissipation is given by

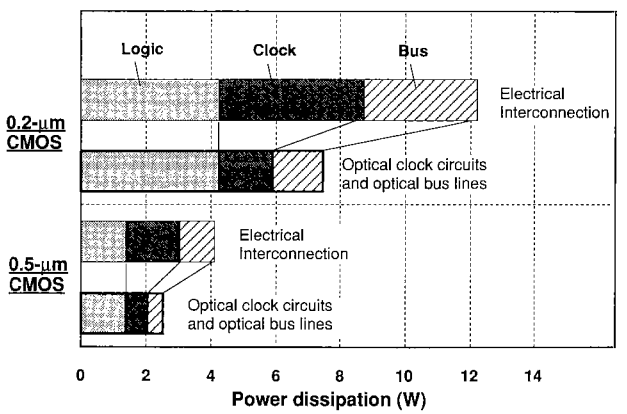
$$P=f_s(C_i+C_w)V_{dd}^2, \quad (1)$$

where f_s is the switching frequency, C_i the sum of the input and output capacitances of a gate, C_w the capacitance of the wire, and V_{dd} the supply voltage. A von Neumann machine comprises internal combination logic, clock distribution circuits, registers, internal buses and I/O buffers, as is shown in Fig. 3. Each circuit operates at a different switching frequency. Although all circuits of the clock distribution and registers operate at the clock frequency, the buses operate at the data-transmission rate, the transition frequency of which is less than half the clock frequency. On the other hand, the operation frequency of the combination logic is considered to be one tenth of the clock frequency.

Let us estimate the power dissipation of each circuit implemented by a 0.5-μm CMOS. If we assume that the supply voltage is 3.3 V, the bus line length is 20 mm, and the number of drivers and detectors is 20, the capacitance of the bus (C_w) is 6 pF per line and the capacitance of the bus drivers and detectors (C_i) is 11 pF. If it operates at 50 MHz, the power dissipation per line is 9.3 mW. If circuits are implemented with a 0.2-μm CMOS and operate at a 1.5 V supply voltage at 125 MHz, the bus line consumes 4.8 mW. The estimated power consumption of the entire chip is shown in Fig. 7, while comparing two design rules. The ratio of the clock circuits and bus power to the total power is larger than 0.5, and it increases with a decrease in the design rule. Although a highly pipelined architecture can greatly improve the processing capability, but it requires a large power dissipation. This means that the product of the machine cycle time and the power dissipation cannot be reduced to the limit. This is the most important limitation regarding the current LSI technology using electrical interconnections.

In order to examine power reduction by optical techniques, the estimated power of the same microprocessor using electrical and optical interconnections are compared in Fig. 7. Optical interconnections are used in the clock distribution circuits and bus lines, where the majority of the global interconnections is used.

A reduction of the power is seen in clock and bus circuits. In these circuits the power is less than half that of the corresponding electric circuits. Microprocessor parameters and device parameters are shown in the tables in Fig. 7. In the case of 0.2-μm CMOS system, four processors are integrated and they are operated at a 250 MHz clock frequency. It is assumed



Processor parameters

Device technology	0.2-μm CMOS	0.5-μm CMOS
No. of processors	4	2
No. of pipeline stages	4	4
No. of Clocks	12	6
No. of buses	6	3
Bus bit width	64 bit	32 bit
No. of bus drivers and detectors	20	20
Clock frequency	250 MHz	50 MHz
Processing capability	4 GOPS	400 MOPS
Total gates	910 Kgates	180 Kgates

GOPS: Giga Operations Per Second
MOPS: Mega Operations Per Second

Device parameters

Device	0.2-μm CMOS	0.5-μm CMOS
Supply Voltage	1.5 V	3.3 V
Ci	0.08 pF/gate	0.16 pF/gate
Cw	0.4 pF/mm	0.3 pF/mm
Power dissipation of optical devices		
Laser + Laser driver	3 mW	
Photo detector + Amplifier	50 μW	

Ci: Gate capacitance
Cw: Interconnection capacitance

Fig. 7 Power dissipation of micro-processor (estimated).

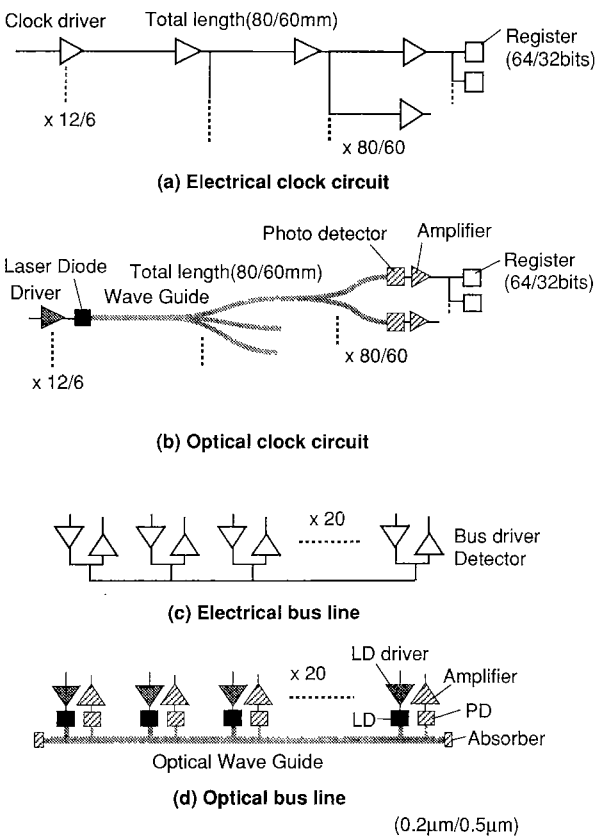


Fig. 8 Block diagram of clock circuit and bus lines.

that the power required for a laser diode (LD) and its driver is 3 mW, and the power for a photo detector (PD) and its amplifier is 50 μW. In order to achieve the low power operation, a non-linear amplifier is used. A class A linear amplifier consumes large power of over 500 μW.

Since there are some unknown parameters, these values are not concrete.

A schematic drawing of the clock circuit and bus line, both optical and electrical ones are shown in Fig. 8. For the clock circuit one LD is used for the master oscillator, light signals are distributed into 80 or 60 PDs. There are 12(6) clock systems will be needed. If one μW is assumed as input for each PDs, one mW laser-light output will be sufficient. For a local distribution of the clock signal, the same circuit as those for electronic clock circuit will be used. In the optical bus line, each register has an LD and its driver connected to an optical wave guide, which serves as a bus line. A PD for each register is also connected to the wave guide. The power required for each LD and its driver is also assumed to be 3 mW. Each PD is loosely coupled with the wave guide and picks up about one μW. A large fraction of the optical power injected into the wave guide is absorbed at both ends of the wave guide in order to avoid multiple reflections.

2. 6 Pin Count and Band-Width Considerations

Another limitation of an electrical interconnection is the number of pins (pin count). According to the empirical Rent Law, the input and output pin count of an ASIC with 100 k gates is about 200~300, that of a 1-M gate ASIC becomes over 1000. Since the wire bonding pitch cannot be made smaller than 100 μm, the maximum number of pins is 500, using wire bonding. Recently, more advanced technologies using tape automated bonding or solder bump bonding have become common. However, these are not still sufficient for processing systems that directly handle two-dimensional data or for neural computers with a very large number of interconnections, like synapses. As it shown in Fig. 5, using the optical interconnection technique for LSIs, it is possible to optical lines directly from spots in a LSI chip to spots in another chip, without having any terminals at pheripheries of these chips. Therefore it will bring drastic impact on the pin count problems discussed above.

Since optical interconnections comprising waveguides, light sources, and photo detectors do not charge and discharge the parasitic capacitance of wiring, the delay time is not limited by the RC delay time or the ringing of an LC line. Therefore, when the performance of existing LSIs using electrical interconnections eventually becomes saturated, optical interconnection technology is expected to offer the following breakthroughs:

(1) Ultra-wide bandwidth interconnections
(2) High speed intra-chip interconnections with low power dissipation

3. Components for Optical Interconnections and Their Characteristics

3. 1 Intrinsic Benefits of Optical Interconnections

In optical interconnections light signal always travel at the speed of light (c/n), whereas in LSI wiring. The electric signal moves much slower, as shown in Fig. 2.

Because light (photon) has no charge, no mutual coupling exists between light signals, whereas electric signals couple with each other, thus creating noise.

The third intrinsic merit of optical interconnections is the potential of significant power reduction. All of the energy of light generated from a light source reaches a photo detector, and hence no intrinsic attenuation exists during travel; whereas the main part of an electric signal will be lost by charging and discharging the wiring capacitor.

The fourth merit of optical interconnections is freedom from "impedance". The impedance of an electric transmission line is too low to match the input or output impedance of small transistors on LSI, the input impedance (voltage/current) of a laser diode, however, can be made so as to have any high value necessary to match those of transistors.

A light signal from an LD can be divided into many PDs without any significant reflection, whereas an output impedance of a transistor of many output loads connected in parallel becomes very low, thus the output wave form is distorted and little power is transmitted into the loads. The interconnection freedom of fan-in or fan-out is an intrinsic advantage of optical interconnections.

Optical interconnections don't require any direct contacts, soldering or connectors all along the pathway. A gap can exist between the LD and the wave guide, a PD and a wave guide without much attenuation, because the light is an electromagnetic wave which can propagate in free space. This is a very

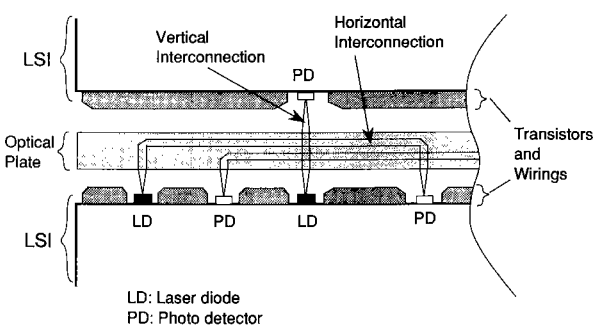


Fig. 9 Structure of "U-OEIC".

important characteristic of the optical interconnection. By using this characteristics many real three-dimensional LSI interconnections can be made. It is difficult to do this with electric interconnections. The new method used for the optical interconnections shown in Fig. 5 and Fig. 9 also uses this characteristics.[7]

3. 2 Optoelectronic Devices for Optical Interconnections

3. 2. 1 Detection Limit of Light Signal

The minimum light power necessary for optical interconnections is determined by statistics. The minimum number of photons to produce sufficiently low error rates (10^{-15} or less) in signal transmission is about 10^4 per pulse. This corresponds to about 1 μW signal power at 1 GHz.[5] Although silicon is also a candidate material, higher performance can be expected by using III-V semiconductors.

An amplifier and its interconnection with PD requires a creative design. To take full advantage of the small amount of light power, the input capacitance of the transistor must be made very small, hopefully of the order of f_F.

3. 2. 2 Light Emitters

Concerning a micron-size laser diode (μ-LDs), there has not yet been any lasers with μA threshold was made. Experiments on small-size surface emitting lasers using highly reflective mirrors and quantum-well active layers, as well as new trials concerning micro-cavity effects, indicate the feasibility of μ-LDs with low thresholds of micro-ampere range.[6] Because of the small size, their response time is expected to be high, tens of GHz or even more. For short-distance optical interconnections, spontaneous light source, light-emitting diode, is applicable. The only concern is the efficiency of the light output. The minimum size of the LD is limited by the light wavelength, which is about one micrometer.

Here again, a concern exists regarding the driving transistor of the μ-LD. To take maximum advantage of high speed, low power optical interconnections, a specially designed transistor driver must be investigated. In this article a 3 mW CMOS driver is assumed to obtain 1 mW light power. Light output efficiency can be made high, when LDs are operated at currant level well above the threshold.

3. 2. 3 Optical Wave-guide Circuits

Based on studies of the U-OEIC Research Group, the most reasonable way to install optical wave guides on an LSI is to make a separate optical substrate, which can accommodate all of the wave guides and associated passive optical components necessary for light interconnection (Fig. 9).

The optical substrate which may be called an "Optical plate", can be fabricated separately from the LSI substrate and its light input and output positions are accurately aligned with LDs and PDs on the LSI substrate. By making a single mechanical alignment with the LSI substrate, the positioning of all active optical components with respect to the passive optical components can be accurately achieved, thus completing the optical interconnection circuit. Eventhough, the basic technologies for an optical plate exist today, intensive research concerning actual design will be necessary.

The optical-plate concept can be applied to an MCM (Fig. 5), however a new technique must be devised for aligning individual chips with respect to the module substrate and to achieve accurate positioning of all the optical components.

3. 4 Fabrication of Optical Interconnections on an LSI

How to install optoelectronics devices into an LSI is a giant challenge. Future optical devices are likely to be made of III-V semiconductors, the LSI will mainly comprise silicon. The fabrication procedure for silicon transistors and optical devices must be compatible. They should not interfere with each other. Studies indicate that all of the processes regarding LSI components, which include metal wiring, is made first while leaving small vacant places (openings) for optoelectronic devices scattered in the sea of transistors. All optoelectronic devices must be constructed afterwards within these vacant spots. The process temperatures of these optoelectronic devices must be made sufficiently low, around 400°C, so as not to disturb the LSI circuit, even one having Al wiring. The results of recent studies on III-V processings indicate its feasibility.

Concerning the hetero epitaxy of highly mismatched materials, GaAs on Si, it is expected that techniques for high-quality epi-layers will be achieved within several years. A flip-chip bonding technique can be used at an early stage of the study when the number of device is small. More details concerning fabrication studies will be reported in elsewhere.[8]

4. Conclusion and Future Prospects

In this article the feasibility of applying optical interconnections, mainly in CMOS microprocessors, is examined. Detailed calculations of delays from the metal wiring and various parts of the circuits are for the first time compared with those using optical interconnections.

The power dissipation of all LSI circuits is also calculated for cases with and without optical interconnections.

These results may not create a startling impression concerning the effect of optical interconnections. However, significant improvements regarding both speed and power is quantitatively demonstrated by this study. Many parameters of optical circuits are still unknown, and somewhat conservative values are used in this analysis. As for LSI circuits, the standard designs of CMOS circuits are used. In order to take full advantage of the optical interconnections, special amplifier circuits will be necessary.

It has also been found that the technique for the optical interconnections of LSIs described here will have significant impact on MCM packages. Not only the speed of signal interconnections, but also the power-reduction effect will be significant, which can only be achieved with the LSI optical interconnections.

It must also be pointed out that these effects can only be obtained by utilizing "intra chip" optical interconnection techniques not by "inter chip" ones. It is also important that such optical interconnections will provide ultra-wide-band chip-to-chip interconnections. The problems of crowded chip periphery will also be relaxed at the same time.

It is important to mention that this new optical interconnection technique for LSIs will certainly have wide range of system applications, not only in single ULSI microprocessors, but also for ultra-parallel multiple-processor systems, neuro-computing systems, image-analyzing systems and many others. There will be many systems which can only be obtained with this LSI optical interconnection technology. This is because the monolithic integration technology of optoelectronic devices with electronic devices will provide basis of these systems, in which a maximum system performance combining light and electronics is expected.[9]

In order for researches to progress regarding this technology, collaboration among people in related fields is essential. Unfortunately, little communication, presently exists between those working in LSI and optoelectronics researches, even among those working in the same electronic research laboratory. According to our experience in the U-OEIC Research group, much useful information exchanging and discussions are stimulated. Those new studies have been exciting and have greatly contributed to progress. It is very important to combine system needs, device ideas and material studies in order to determine the best direction to proceed.

Optical interconnections in an LSI are not an easy task, and hence much innovative work and many breakthroughs are necessary in related fields. Since it will take many years to reach even the starting point for real applications, this kind of communication between people in related fields must start immediately. Nothing will happen without this.

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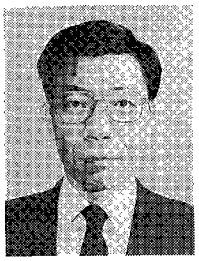

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