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New Non-Volatile Analog Memory Circuits Using PWM Methods

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SUMMARY This paper proposes non-volatile analog memory circuits using pulse-width modulation (PWM) methods. The conventional analog memory using floating gate device has a trade-off between programming speed and precision because of the constant width of write pulses. The proposed circuits attain high programming speed with high precision by using PWM write pulses. Three circuits are proposed and their performance is evaluated using SPICE simulation. The simulation results show that fast programming time less than 20 μs, high updating resolution of 11 bits, and high precision more than 7 bits are achieved.

key words: *analog memory, floating gate device, pulse width modulation, PWM*

1. Introduction

Although many VLSI digital storage techniques have been developed, direct analog storage or multi-level digital data storage is more effective in such applications as voice recording [1], [2], neural networks [3] or multi-valued logic systems. Multi-level programming in flash memory is also recognized as a technique for high-density mass storage [4]–[6].

There are three approaches to store analog data; one is using charges stored in capacitors, another is using floating-gate devices, and the other is using ferroelectric materials.

The first approach is generally used in analog circuits as sample-and-hold circuits. It is also used in LSI implementation of neural networks [7]. However, analog data cannot be retained for long time because of leakage current. Since the retention time is at most a few seconds [7], this approach cannot be applied to all applications.

Ferroelectric memory in the third approach is very promising for high-speed non-volatile analog storage devices [8] as well as digital ones [9]. The programming time is expected to be on the order of nano-seconds. However, much more work needs to be done before it can be adopted in the practical LSI fabrication process.

Floating-gate devices can retain analog data for long time and they are the only practical non-volatile analog memory in the present LSI technology. Therefore, many analog memory circuits and devices using floating-gate structures have been proposed [1], [2], [10]–[18]. In these works, most programming circuits for the conventional floating-gate structure use feedback control in the programming loop consisting of write and read/verify periods [1], [2], [6]. Although these methods can apply to the conventional flash EEPROM cells, they have a trade-off between programming speed and precision because of using write pulses having a constant voltage and width. For example, programming time of a few hundred microseconds is required for achieving 6 to 8 bit precision [6], [18].

Some new non-volatile memories that realize simultaneous read/write operation have been proposed. One idea is adding an auxiliary capacitive-coupling gate compensating for effects of write pulses [16], but a larger cell size is required, and programming time is still long [18]. Another idea uses neuron-MOS comparator [17], which may achieve high speed programming although the programming can performs only in one direction.

In this paper, we propose analog memory using PWM write pulses. Because the PWM signal can vary the pulse width, we attain fast programming speed with high precision although we use the conventional feedback control scheme. The programming circuits can update memory in both incremental and decremental directions, and they also attain high updating resolution, which is important for application to neural networks [3]. In Sect. 2, after the principle of programming control is presented, three programming circuits are proposed, and their operations are explained. In Sect. 3, HSPICE simulation results of our analog memory circuits are shown, and finally the conclusion is given in Sect. 4.

2. Analog Memory Circuits

2.1 Programming Control Using PWM Signals

The principle of the programming operation is shown in Fig. 1. The comparator compares the stored data in the memory, V_{OUT}, with the target data, V_{TAR}, and output the difference with a PWM signal. The memory device changes V_{OUT} using the PWM signal.

During the period of PWM difference signal, the

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floating-gate device updates its memory by the write pulse. For the large difference, a large updating is performed because the width of write pulse is wide. Therefore, the programming time can be shortened compared with the conventional schemes because the number of verification decreases. On the other hand, for the small difference, a small updating is performed because the width of write pulses is narrow. If ideal PWM signals can be generated, longer programming time leads higher precision in this method. In the conventional schemes, on the contrary, write precision is limited by the constant pulse width, irrespective of long programming time.

There are two approaches to make a PWM difference pulse from two voltages V_{OUT} and V_{TAR}.

- approach-A: two voltages V_{OUT} and V_{TAR} are converted to PWM signals, respectively, and then the difference pulse of the two PWM signals is generated using logic gates as shown in Fig. 2.
- approach-B: the voltage difference is obtained from V_{OUT} and V_{TAR}, and then the voltage difference is converted to the PWM difference pulse.

On the basis of these two approaches, we propose two types of circuits.

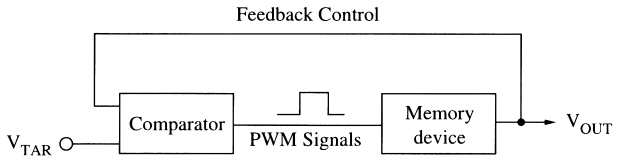

Fig. 1 Principle of programming control.

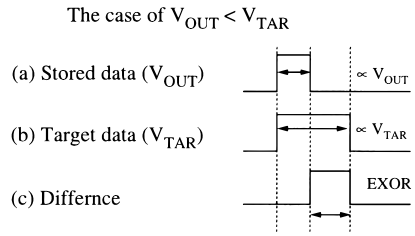

Fig. 2 PWM signals generated for programming control.

2.2 Circuit-A: Using the Difference of PWM Signals

An analog memory circuit based on approach-A is shown in Fig. 3. This circuit consists of two voltage-to-width converters (VWC's), logic gates that calculate the difference of PWM pulses (DIF), a floating-gate device, and high-voltage switches (HVSW's).

The circuit operation is as follows: in the upper VWC, during period T_1, switches S_1 and S_2 are closed, and capacitor C_1 holds the voltage of the difference between V_{OUT} and the threshold voltage of the inverter in the VWC. During period T_2, switch S_3 is closed, and a ramped voltage waveform (Ramp) is inputted. A PWM signal having a width proportional to V_{OUT} appears at node n_1. In the lower VWC, a PWM signal having a width proportional to V_{TAR} appears at node n_2.

A PWM signal having a width of the difference of above two PWM signals is generated by DIF. For $V_{OUT} < V_{TAR}$, the PWM difference signal appears at node n_3, and high voltage V_{ppg} is supplied to the control gate of the floating-gate device during the PWM pulse. Electrons are injected into the floating-gate and the potential of the floating-gate is lowered. Therefore, V_{OUT} increases and approaches V_{TAR}. On the other hand, for $V_{OUT} > V_{TAR}$, the PWM difference signal appears at node n_4. V_{OUT} decreases and approaches V_{TAR}. By repeating this operation, V_{OUT} becomes equal to V_{TAR}.

This circuit can receive a PWM signal at node n_2 as the target signal instead of V_{TAR}, and can output

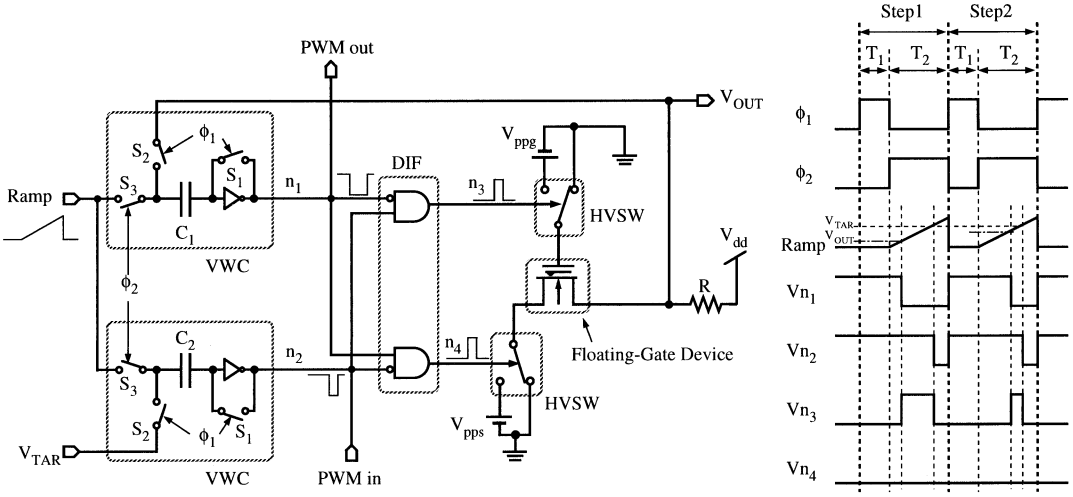

Fig. 3 Analog memory circuit-A and the timing diagram when $V_{OUT} < V_{TAR}$.

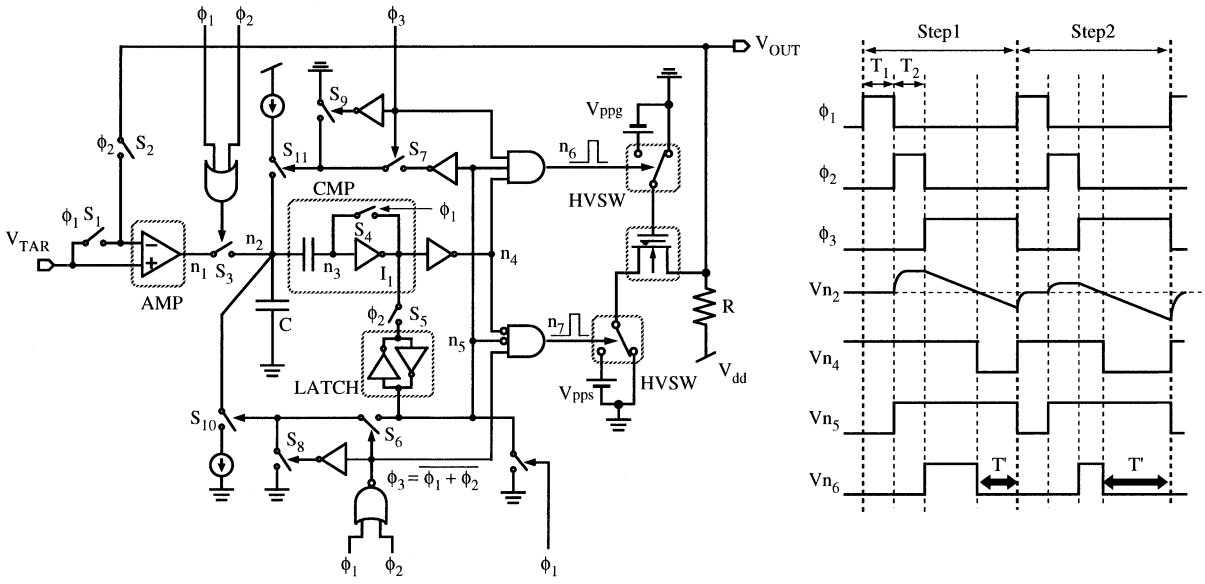

Fig. 4 Analog memory circuit-B and the timing diagram when $V_{OUT} < V_{TAR}$.

a PWM signal from node n_1 as a memory output instead of V_{OUT}. This feature matches the analog-digital merged architecture using PWM pulses proposed by the authors [19].

2.3 Circuit-B: Using PWM Pulses Converted from the Voltage Difference

Figure 4 shows an analog memory circuit based on the approach-B. This circuit consists of a differential amplifier (AMP), a comparator (CMP), a latch circuit (LATCH), a floating-gate device and high voltage switches. The characteristic of AMP is shown in Fig. 5. The gain is not so high and the output gradually changes in the transition region.

This nonlinear characteristic is effective for fast programming under the condition of the limited output range. When the difference between V_{OUT} and V_{TAR} is large, the amplifier operates in region α_1 or α_2, and the output voltage is a large constant value. Therefore, the update value is large and V_{OUT} approaches V_{TAR} more quickly than in circuit-A. When the difference between V_{OUT} and V_{TAR} is small, the amplifier operates in region β, and the amplifier output voltage is proportional to the difference. Therefore, V_{OUT} approaches V_{TAR} precisely.

The operation of this circuit is as follows. First, by clock ϕ_1, switches S_1, S_3 and S_4 are closed. Both inputs of the amplifier are V_{TAR} and node n_3 is set at the threshold voltage of inverter I_1. This operation compensates the offset of inverter I_1. Second, switches S_1 and S_4 are opened, and switches S_2, S_3 and S_5 are closed by clock ϕ_2. Voltages V_{OUT} and V_{TAR} are fed into AMP, and Node n_1 and n_2 are set at the output voltage of AMP. If $V_{OUT} < V_{TAR}$, capacitor C is charged up. Comparator CMP detects which larger V_{OUT} or V_{TAR} is, and LATCH holds this information. In this case, the output of LATCH holds "High."

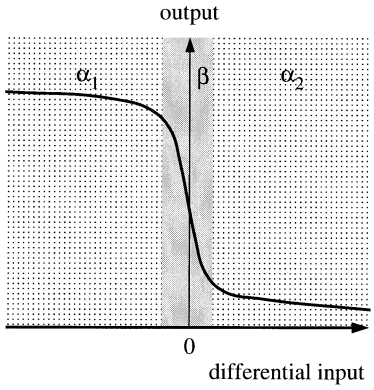

Fig. 5 Characteristic of the differential amplifier.

Third, switches S_2, S_3 and S_5 are opened and switches S_6 and S_7 are closed by clock ϕ_3. Since node n_5 is set at "High," switch S_{10} turns on. Capacitor C is connected to the current source and discharged. Thus, the voltage of node n_2 lowers, and then inverter I_1 inverts. As a result, a PWM signal appears at node n_4. This PWM signal and the output of LATCH make a PWM write pulse at node n_6. Thus, voltage V_{ppg} is supplied to the control gate of floating-gate device during the period of the PWM write pulse, and V_{OUT} rises and approaches V_{TAR}.

On the other hand, if $V_{OUT} > V_{TAR}$, capacitor C is initially discharged. node n_5 is set at "Low" and switch S_{11} turns on. Capacitor C is charged up, and then a

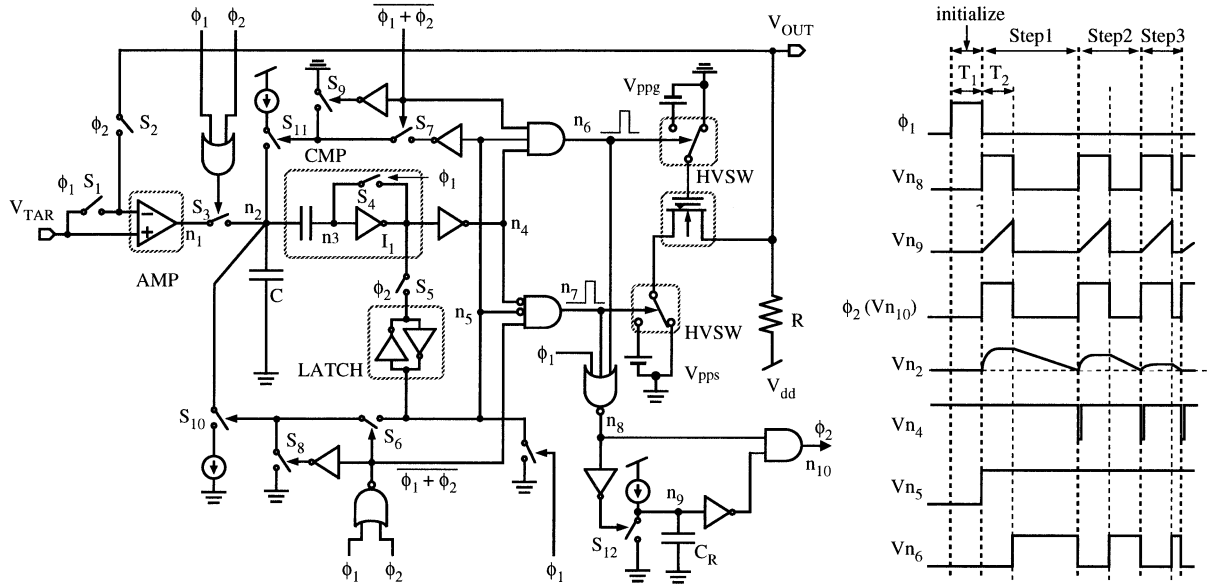

Fig. 6 Analog memory circuit-B′ and the timing diagram when $V_{OUT} < V_{TAR}$.

PWM write pulse appears at node n_7. Voltage V_{OUT} lowers and approaches V_{TAR}. Finally V_{OUT} becomes equal to V_{TAR} by repeating this operation.

As shown in the timing diagram in Fig. 4, this programming operation is synchronous with clock ϕ_1 and the interval of operation steps is constant. This is suitable for programming for the memory cell array. However, when the PWM write pulse is short, this circuit has to wait for the next write operation step during period T'. If the circuit moves to the next write operation step at once when the PWM write pulse ends, whole programming operation finishes more quickly. This operation is achieved by an autonomous asynchronous circuit. Such a circuit is described in the next section.

2.4 Circuit-B′: Asynchronous Updating for Faster Programming Operation

Figure 6 shows an asynchronous updating circuit and the timing diagram. We add a new circuit block for detecting the end of each write operation step. This block generates clock signal ϕ_2 for programming control. The offset compensation operation triggered by clock ϕ_1 is performed only once at the first step of whole programming operation. When there is no write pulse at both node n_6 and n_7, capacitor C_R is connected to the current source and is charged up. A pulse appears at node n_{10} and it is used as clock ϕ_2.

3. Simulation Results

We carried out HSPICE simulation of the proposed circuits. The equivalent circuit of the floating-gate device was assumed as shown in Fig. 7. The equivalent circuit consists of an NMOSFET, two capacitors and a

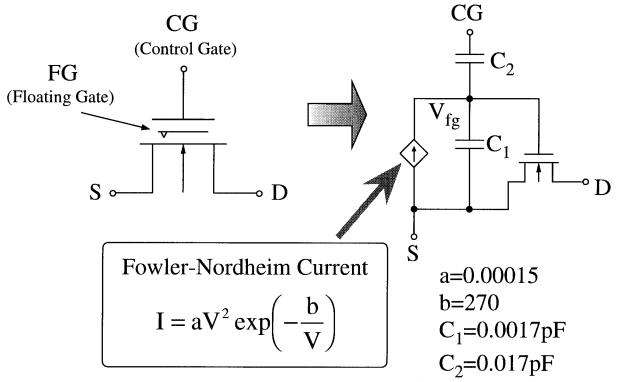

Fig. 7 An equivalent circuit of the floating-gate device.

voltage controlled current source expressing the Fowler-Nordheim current. We used the values of a and b assumed in Ref. [13], which were extracted from a 1.5 μm EEPROM process. The device parameters of the programming circuits were based on a 0.6 μm CMOS process. The HVSW was composed of an NMOS switch. It was assumed that $V_{dd} = 3.3$ V and $R = 50$ kΩ.

Figure 8(a) shows a simulation result of circuit-A, where $V_{ppg} = V_{pps} = 21$ V, the initial value of V_{OUT} is 0.6 V, and V_{TAR} is changed from 2.0 V to 0.6 V 30 μs after the programming starts. This is the worst case of the programming speed when the permissible error is determined by the way mentioned below. Figure 8(b) shows the magnified waveform of V_{OUT} around $t = 38\,\mu$s. Periods T_1 and T_2 correspond to those in the timing diagram shown in Fig. 3. A PWM signal appears in period T_3, and V_{pps} is supplied to the floating-gate device. After supplying V_{pps}, V_{OUT} approaches V_{TAR}. At the beginning of the programming, the write pulse

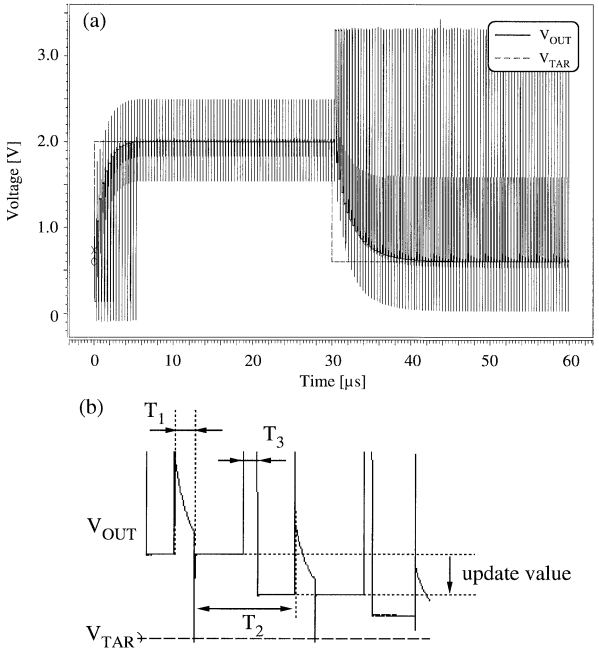

Fig. 8 Simulation result of circuit-A.

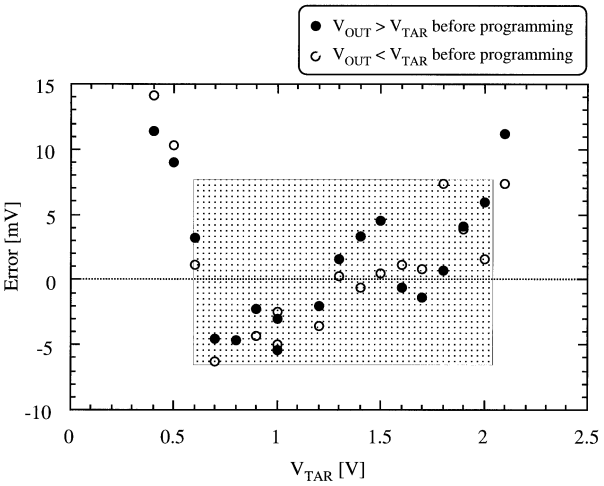

Fig. 9 Setting error of V_{OUT} in circuit-A.

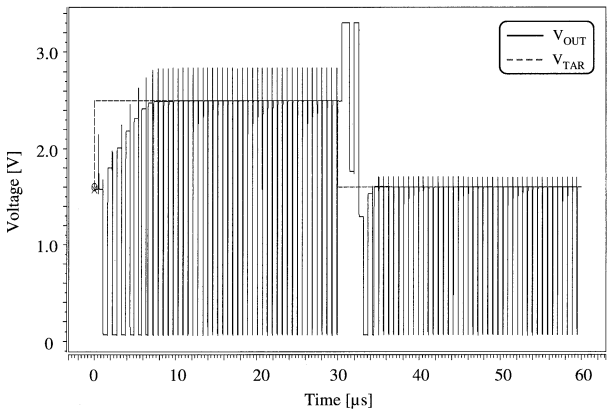

Fig. 10 Simulation result of circuit-B′.

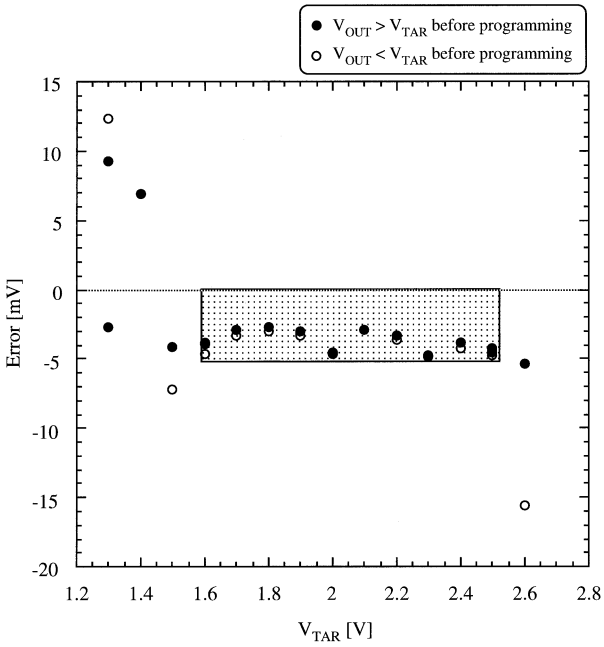

Fig. 11 Setting error of V_{OUT} in circuit-B′.

width is wide and the updating value is large because the difference between V_{OUT} and V_{TAR} is large. Therefore, V_{OUT} approaches V_{TAR} quickly. The smaller the difference between V_{OUT} and V_{TAR} is, the smaller the updating value is.

Figure 9 shows the setting error of V_{OUT} as a function of V_{TAR}. The error is the largest value during the programming period of 50 μs. If the permissible error is assumed $\pm$ 7.0 mV, the controllable range is from 0.6 V to 2.0 V. Because the full range of V_{OUT} is 1.4 V, the maximum setting error is $\pm$ 0.50 %, which means 6.6 bits precision.

The programming time depends on the initial value of V_{OUT} and V_{TAR}. If the programming time is defined as the time when the setting error first becomes below the permissible value in the worst case, it is 20 μs in circuit-A. At that moment, the minimum updating resolution is about 11 bit.

Figure 10 shows a simulation result of circuit-B′, where V_{ppg} = 18 V, V_{pps} = 20 V, the initial value of V_{OUT} is 1.6 V, and V_{TAR} is changed from 2.5 V to 1.6 V 30 μs after the programming starts. This is also the worst case of programming speed. At the first step of whole writing operation, the offset compensation operation is performed. After this operation, V_{OUT} approaches V_{TAR} quickly, and the updating value becomes very small after 8 μs. In order to achieve fast and high-precision programming, we performed asymmetric programming by setting $V_{ppg} \neq V_{pps}$; i.e. the update rate was set large when $V_{OUT} > V_{TAR}$, and it was set

small when $V_{OUT} < V_{TAR}$. Therefore, V_{OUT} always approach V_{TAR} under the condition that $V_{OUT} < V_{TAR}$ as shown in Fig. 10.

Figure 11 shows the setting error of V_{OUT} as a function of V_{TAR}. The error is the largest value during the programming period of 30 μs. If the permissible error is assumed -5.0 mV, the controllable range is from 1.6 to 2.5 V. Because the full range of V_{OUT} is 0.9 V, the maximum setting error is -0.56%, which means 7.5 bits precision.

The programming time is 14 μs in circuit-B$'$ if the same definition as in circuit-A is used. Although V_{ppg} and V_{pps} are lower than those in circuit-A, the programming time is short.

4. Conclusion

We proposed three analog memory circuits using PWM write pulses generated by the feedback control loop. In the first one (circuit-A), the stored voltage data and the target voltage data are converted to PWM pulses, respectively, and the difference of pulse widths in both PWM pulses is generated. The simulation results show the programming time for achieving 6.6 bit precision is about 20 μsec, which is much faster compared with the conventional analog memory circuits. The remarkable feature of circuit-A is that it can output the stored data as a PWM pulse, which matches the analog-digital merged architecture using PWM pulses.

The second and third circuits (circuit-B and -B$'$) use PWM write pulses converted from the voltage difference between the stored data and the target one. Because of removing the extra periods, the programming speed of these circuits is faster than that of circuit-A. In addition, by performing asymmetric programming, they can achieve more accurate programming. Since circuit-B is a synchronous version and circuit-B$'$ is an asynchronous version, circuit-B$'$ is faster than circuit-B. The simulation results show that circuit-B$'$ can achieve 7.5 bit precision in 14 μsec.

An EEPROM cell array structure can be used in these memory circuits. However, two select transistors should be required per cell because both *write* and *erase* updates can be performed for programming a cell.

Since the non-volatile analog memory circuits proposed in this paper attain high programming speed with high precision and update resolution, they can be applied to various LSI systems which perform analog processing.

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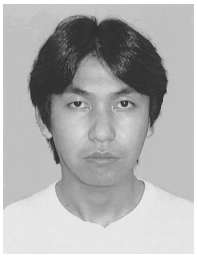

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