

An Hadamard Transform Chip Using the PWM Circuit Technique and Its Application to Image Processing

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SUMMARY A circuit that carries out an Hadamard transform of an input image using the pulse width modulation technique is proposed. The proposed circuit architecture realizes the function of an Hadamard transform with a full-size pixel image. A test chip that we designed and fabricated integrates 64×64 pixels in a $4.9 \text{ mm} \times 4.9 \text{ mm}$ area, with $0.35 \mu\text{m}$ CMOS technology. The functional operation and linearity of this chip are measured. An image processing application utilizing this chip is demonstrated.

key words: *Hadamard transform, image sensor, pulse width modulation technique, charge sharing*

1. Introduction

Among the many kinds of orthogonal transformations, discrete cosine transform (DCT) has been applied to the compression of natural images. On the other hand, the Hadamard transform is used for implementation of image coding because it does not require real number multiplication [1]. Because transforming large images requires power dissipation, chip area, accuracy and processing time, the data for such images are usually divided into small sub-blocks (e.g. 16×16) and then transformed. However, dividing an image into sub-blocks restricts the processing of the image. For example, a spatial low-pass filter frequency is limited to sub-block size.

In order to overcome these restrictions, we propose a novel Hadamard transform circuit that can entirely transform large-size images. To solve the problems of power dissipation and chip area, we adopt a pulse width modulation (PWM) technique because it depresses the frequency of signal changing more than a digital circuit does, and because PWM circuit elements are compact [2]–[4]. To solve the accuracy problem, we adopt a charge-sharing scheme, preventing corruption of the circuit during calculation [5]. To solve the problem of time consumption, parallel calculation using the PWM circuit is effective [6].

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A digital circuit, such as that of a fast Hadamard transform, also achieves speed and accuracy. However, this would require the conversion of each pixel into a digital value through an analog-to-digital converter (ADC). In the circuit we propose, on the other hand, the Hadamard transform function can be applied to a chip image sensor, because the circuit can deal with analog values directly.

The artificial retina chip realizes orthogonal transforms to detect features, but it can do only one-dimensional transforms [7].

In this paper, we propose a circuit that performs an entire Hadamard transform. The proposed circuit not only compresses images but detects shapes and features, and it would be applicable to intelligent machine vision systems.

2. Hadamard Transform Circuit

2.1 Hadamard Transform and Inverse Hadamard Transform

The Hadamard transform is achieved by calculating correlation values of an image matrix and Hadamard bases.

One-dimensional (1-D) Hadamard bases are obtained recursively by Eq. (1).

$$H_N = H_{N/2} \otimes H_2 \quad H_2 = \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix} \quad (1)$$

Where N is a base size and \otimes is a Kronecker multiplication. When $N = 8$,

$$H_8 = \begin{bmatrix} 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\ 1 & -1 & 1 & -1 & 1 & -1 & 1 & -1 \\ 1 & 1 & -1 & -1 & 1 & 1 & -1 & -1 \\ 1 & -1 & -1 & 1 & 1 & -1 & -1 & 1 \\ 1 & 1 & 1 & 1 & -1 & -1 & -1 & -1 \\ 1 & -1 & 1 & -1 & -1 & 1 & -1 & 1 \\ 1 & 1 & -1 & -1 & -1 & -1 & 1 & 1 \\ 1 & -1 & -1 & 1 & -1 & 1 & 1 & -1 \end{bmatrix} \quad (2)$$

Each column is a 1-D Hadamard base and is replaced in the order of the frequency.

$$\begin{bmatrix} W_1 \\ W_2 \\ W_3 \\ W_4 \\ W_5 \\ W_6 \\ W_7 \\ W_8 \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\ 1 & 1 & 1 & 1 & -1 & -1 & -1 & -1 \\ 1 & 1 & -1 & -1 & -1 & -1 & 1 & 1 \\ 1 & 1 & -1 & -1 & 1 & 1 & -1 & -1 \\ 1 & -1 & -1 & 1 & 1 & -1 & -1 & 1 \\ 1 & -1 & -1 & 1 & -1 & 1 & 1 & -1 \\ 1 & -1 & 1 & -1 & -1 & 1 & -1 & 1 \\ 1 & -1 & 1 & -1 & 1 & -1 & 1 & -1 \end{bmatrix} \quad (3)$$

The two-dimensional (2-D) Hadamard bases are made using the 1-D Hadamard bases;

$$W_{ij} = W_i^T W_j \quad (4)$$

Correlation values c_{ij} between Hadamard bases W_{ij} and an image matrix F are obtained as follows:

$$c_{ij} = \frac{W_{ij} \oplus F}{N^2} \quad \left(A \oplus B = \sum_{l,m} a_{lm} b_{lm} \right) \quad (5)$$

An element of correlation values c_{ij} is called an Hadamard coefficient. Similarly, an inverse Hadamard transform is calculated using Hadamard coefficients c_{ij} and Hadamard bases W_{ij} .

$$F = \sum_{i,j} c_{ij} W_{ij} \quad (6)$$

Figure 1 shows 2-D Hadamard bases when $N = 8$. In Fig. 1 and throughout this paper, the white area represents +1 and the black area represents -1. As the figure shows, the frequency increases from the left upper side to the right bottom side. All elements of W_{11} are +1.

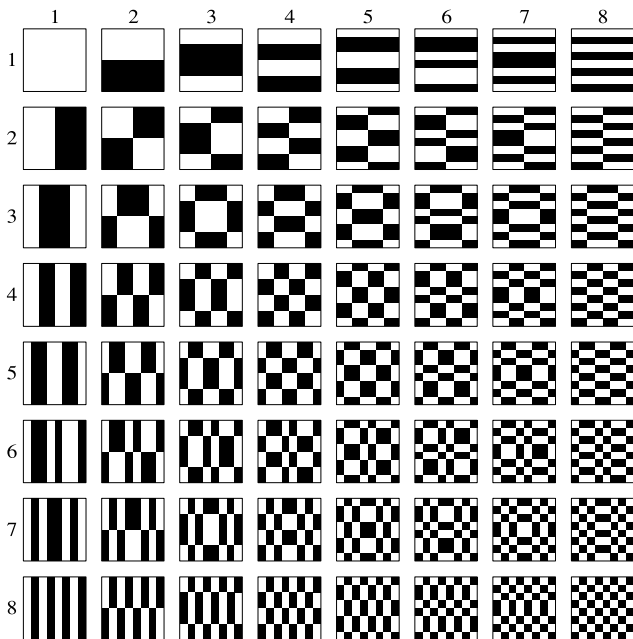


Fig. 1 2-D Hadamard bases ($N = 8$).

Figure 2 shows examples of the Hadamard transform and of the inverse Hadamard transform. Figure 2(b) shows Hadamard coefficients made from the original image (Fig. 2(a)) without image division to sub-blocks. As shown in Fig. 2(b), the power concentrates in the left upper part. Using these coefficients of the left upper part, the image can be reconstructed (Figs. 2(c)–(f)).

2.2 Pulse Width Modulation Technique

The analog-digital merged circuit architecture using PWM approaches is applied to a basic processing circuit.

Figure 3(a) shows an optical-to-PWM (O-to-PWM) converter. The capacitor C_p , which works as an analog memory for non-destructive readout, is charged to the threshold of the comparator (Comp). The photo detector (PD) works as a current source, which is proportional to pixel intensity, and discharges from capacitor C_p . The voltage of node C_p is increased by the application of ramped voltage. The comp compares this voltage with its own threshold and outputs a PWM

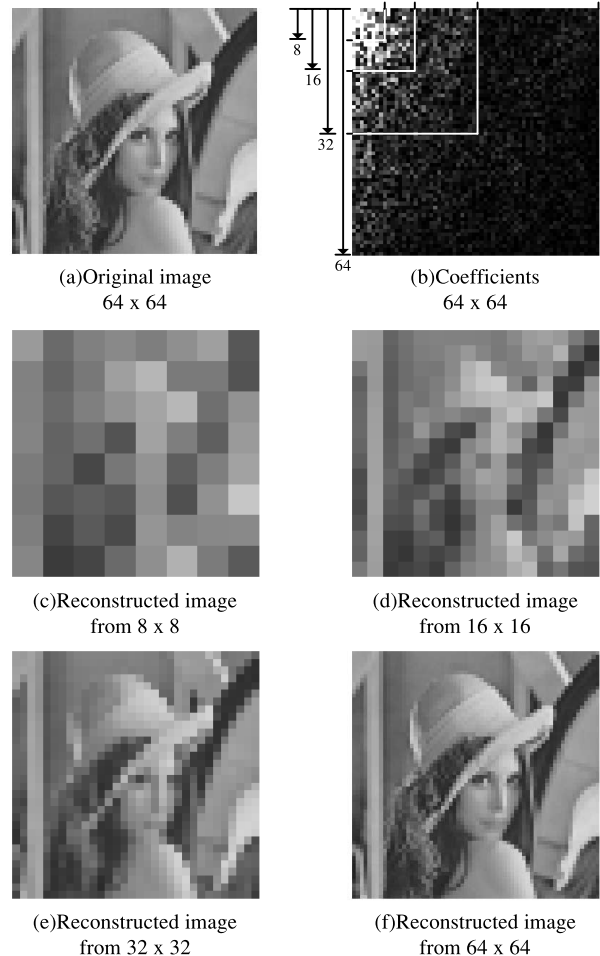


Fig. 2 Hadamard transform and Inverse Hadamard transform.

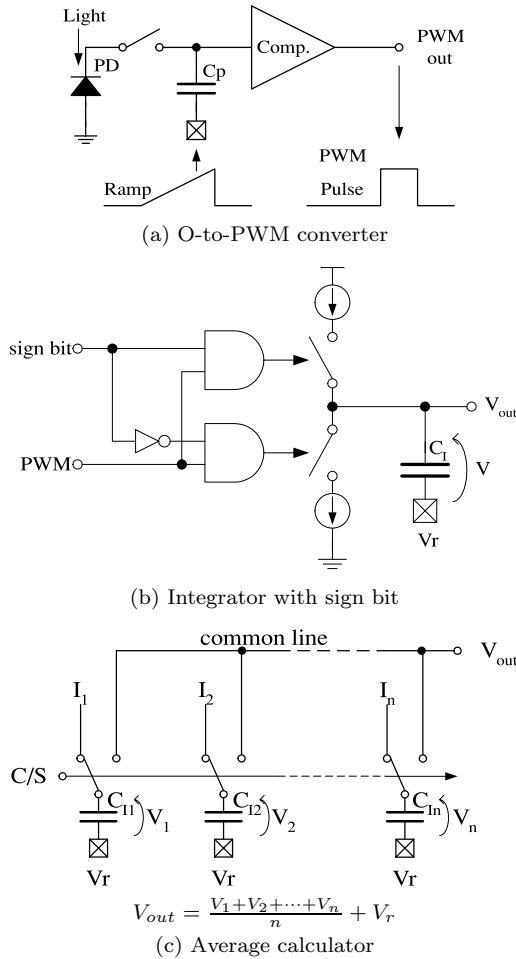


Fig. 3 Pulse width modulation technique elements.

signal.

Figure 3(b) is an integrator with a sign bit. Either switch is closed by a PWM signal selected by the sign bit. This circuit calculates PWM signal input corresponding to the sign bit.

Figure 3(c) is an average calculator. Each capacitor C_{I_i} integrates current I_i during the charge/share control signal (C/S) is “C.” During C/S is “S,” all of the capacitors are connected to common line and share charges. This circuit calculates average voltage V_{out} biased by a reference voltage V_r .

2.3 Hadamard Transform Circuit

We propose a Hadamard transform circuit.

Figure 4 is a block diagram of our Hadamard transform circuit. This circuit is composed of two Hadamard transform base generators, an array of cells and an ADC. The Hadamard base generators provide cells with 1-D Hadamard bases from row and column. All cells connect to a common line. The ADC converts the voltage of the common line to digital data.

Figure 5(a) is an Hadamard transform base generator when $N = 8$. To input the base number as a gray

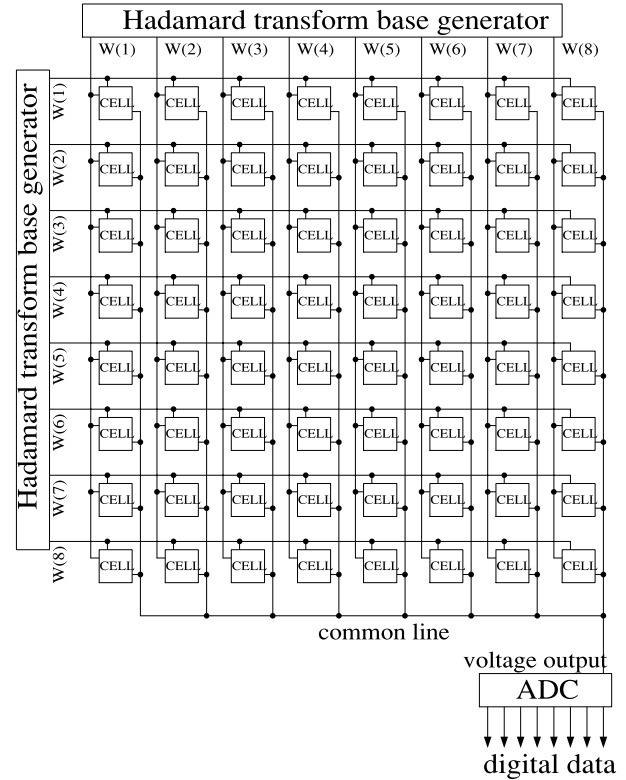


Fig. 4 Block diagram of Hadamard transform circuit.

code G , this generator generates 1-D Hadamard base W . Another base size can be easily analogized from this schematic.

Figure 5(b) is a circuit schematic of the cell. This circuit is composed of the PWM processing circuits described in Sect. 2.2. Ex-Nor calculates a 2-D Hadamard base element using the 1-D Hadamard base elements from row and column (cf. Eq. (4)). A 2-D Hadamard base element with a bipolar state $+1$ or -1 works a sign bit. The O-to-PWM converter outputs the PWM signal, which corresponds linearly to pixel intensity. The capacitor $C_{I_{ij}}$ integrates the charge depending on the PWM signal and sign bit. All charges are shared by closing all switches (S_{ij}) and are averaged instantaneously.

The circuits shown in Figs. 4 and 5 also realize an inverse Hadamard transform (cf. Eq. (6)). Each cell is provided with the PWM signal simultaneously corresponding to Hadamard coefficients c_{ij} instead of the O-to-PWM output. Capacitors $C_{I_{ij}}$ integrate the coefficients multiplied by 2-D Hadamard base elements. These capacitors $C_{I_{ij}}$ perform summation by providing all coefficients c_{ij} sequentially and reconstruct pixels. The reconstructed pixel values are read out by closing S_{ij} sequentially.

2.4 Circuit Simulation of Basic Operation

Figure 6 shows simulated waveforms of V_{ij} with 2×2

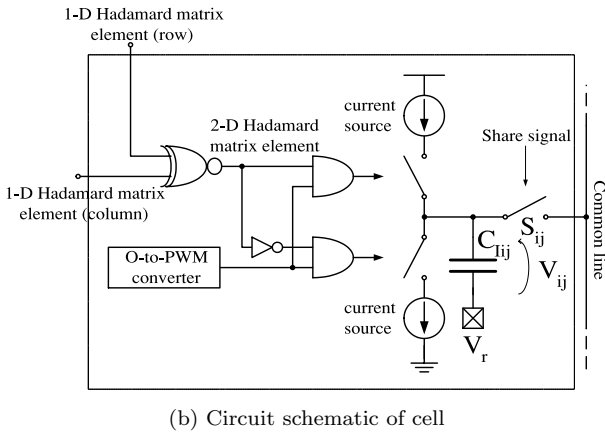
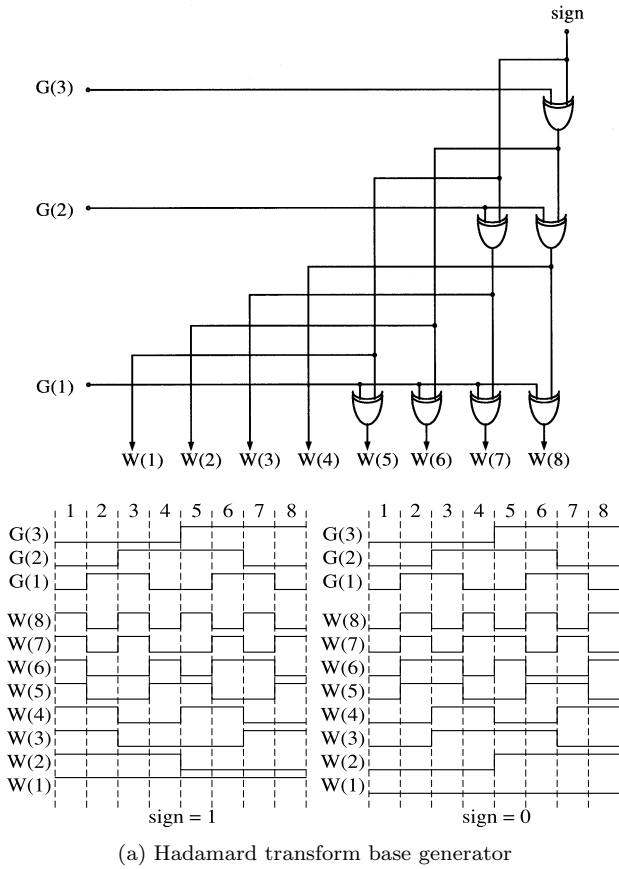


Fig. 5 Hadamard transform circuit elements.

cells. Input PWM pulse width and 2-D Hadamard base elements were set to $(1 \mu s, +1)$, $(1 \mu s, -1)$, $(0.5 \mu s, +1)$ and $(0.5 \mu s, -1)$. The charging terms are those from 0 s to $1 \mu s$, and the sharing terms are those after $1 \mu s$. This simulation verified charging and sharing operations.

For SPICE simulation, the standard Lena image with a reduced resolution of 32×32 is applied to the Hadamard transform circuit. To change an Hadamard base sequentially ordering shown in Fig. 7(a), the circuit outputs each coefficient corresponding to the base. Figure 7(b) shows values of coefficients calculated by

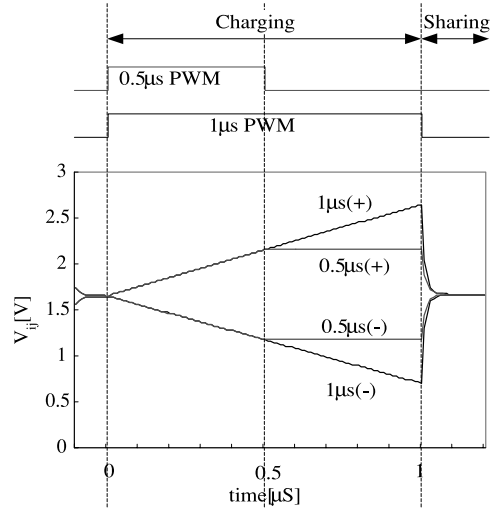


Fig. 6 SPICE simulation results (charging and sharing).

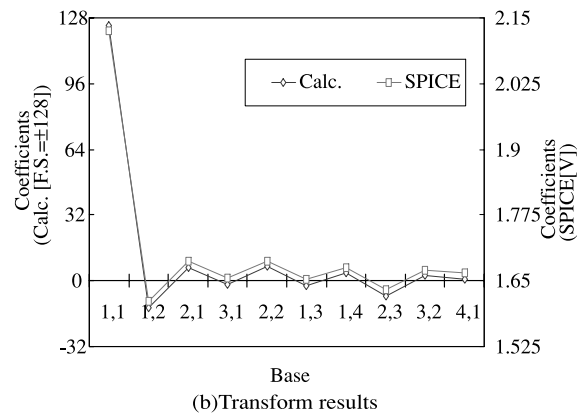
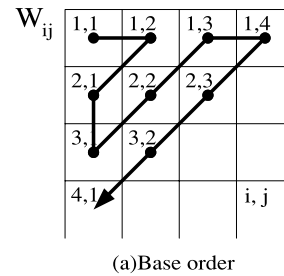


Fig. 7 Comparison between calculation and SPICE simulation.

numerical calculation (Calc.) and SPICE simulation (SPICE). Accuracy is estimated as the difference between the Calc. scaled voltage and the SPICE voltage divided by the full scale of voltage. The two are in good agreement, with an accuracy of more than 7 bits.

3. Test Chip Design and Evaluation

3.1 Chip Design

We designed a test chip to confirm that the Hadamard transform circuit would perform in an actual chip.

The Hadamard transform circuit contains PDs and capacitors. The PD needs at least $200 \mu\text{m}^2$ for light sensitivity (maximum current is 0.05 nA). The sample capacitor C_p needs at least 0.3 pF to tolerate current leakage and noise. The share capacitor C_I needs 0.8 pF to ignore parasitic capacitance of the common line. The parasitic capacitance of the common line is estimated to be about 14 pF . Capacitors C_p and C_I require chip areas of $160 \mu\text{m}^2$ and $420 \mu\text{m}^2$, respectively. Based on these chip area estimations, a cell is able to array 64×64 on a $4.5 \text{ mm} \times 4.5 \text{ mm}$ chip. (When charge sharing, total share capacitance is 250 times larger than the parasitic capacitor.)

This test chip consisted of 64×64 cells (CELL), two base generators with a shift register (DFF) to control the charge sharing signal, and an output buffer (FOL).

The estimated power consumption of this chip using SPICE is 178 mW at a 3.3 V supply. Specifications are shown in Table 1.

To enhance application fields, resolution must be

Table 1 Specifications.

Technology	0.35 μm CMOS, 3Al, 2Poly-Si	
Power Supply	3.3 V	
Power Dissipation	178 mW	
Fill Factor	6%	
Number of Pixels	64×64	
Chip Size	CELL	$55 \mu\text{m} \times 55 \mu\text{m}$
	DFF	$55 \mu\text{m} \times 66.6 \mu\text{m}$
	FOL	$321 \mu\text{m} \times 120.25 \mu\text{m}$
	ALL	$4.5 \text{ mm} \times 4.5 \text{ mm}$
Number of Transistors	CELL	48 tr.
	DFF	46 tr.
	FOL	200 tr.
	ALL	202696 tr.
PWM Signal Accuracy	7 bits	
Readout Time	4.096 ms	
Dynamic Range	33.3 dB	

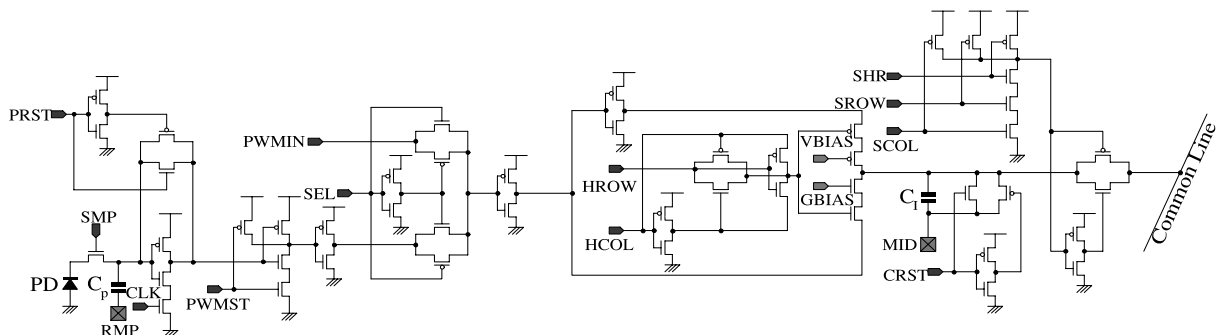
higher than about 256×256 pixels. To realize such high resolution, we have to reduce the pixel size, which is dependent on the photo detector, the sample capacitor and the shared capacitor. Accuracy is determined by using the ratio of parasitic capacitance on the common line for charge share to the sum of the shared capacitors. If we use a $0.35 \mu\text{m}$ CMOS process, the estimation value of the parasitic capacitor is 36 pF and share capacitance is almost $0.13 \mu\text{F}$ ($256 \times 256 \times 0.2 \text{ pF}$). The ratio of share capacitance to parasitic capacitor is 360. The parasitic capacitors decrease with minimum feature size. Therefore, we can decrease the size of shared capacitor as we decrease the minimum feature size. This shows that this circuit architecture is suitable for use in a high-resolution Hadamard transform chip.

Figure 8 shows a cell constituted by CMOS. For implementation, several brand-new signals have been added. PRST resets C_p to the threshold of the comparator. SEL selects an external (PWMIN) or internal PWM signal. PWMIN is used for inverse Hadamard operation. SROW and SCOL connect to the shift register located in each row and column. SROW and SCOL select which capacitor C_I to share. SROW and SCOL are used when reading C_I directly and when making exotic bases. CRST resets C_I and the common line to MID. Figure 8 also provides the meaning of each signal.

A top view of the layout is shown in Fig. 9. What appears as a geometric pattern is CELL array. CELL array occupies most of the chip's area. Two DFF arrays are located along upper and left edge. FOL is located at the bottom left. ADC is equipped outside of this test chip.

3.2 Evaluation

In order to evaluate the function of this Hadamard



PRST	sample capacitor C_p ReSeT	SMP	SamPle optical input
RMP	RaMP Input	CLK	CLoCK for comparator
PWMST	PWM STrart	PWMIN	external PWM Input
SEL	SElect external / internal PWM	HROW	Hadamard base element from ROW
HCOL	Hadamard base element from COLumn	SHR	SHaRe signal
VBIAS	Vdd side BIAS for current source	GBIAS	Gnd side BIAS for current source
SROW	Shift register input from ROW	SCOL	Shift register input from COLumn
MID	MIDdle voltage supply	CRST	Charge share capacitor C_I reset

Fig. 8 Cell.

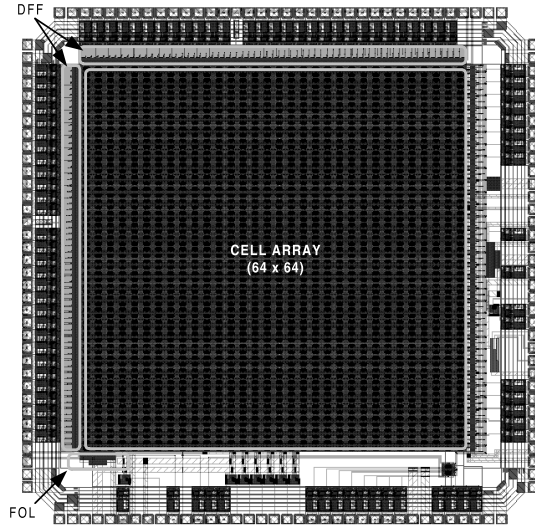


Fig. 9 Layout of Hadamard transform chip.

transform chip, a measurement method is devised. The image applied to the chip is fixed as shown in Fig. 10(c), and Hadamard bases are changed sequentially as shown in Fig. 10(a).

Figure 10(b) shows the outputs versus Hadamard bases as they change with time. In this measurement, about 30% of the light power passes through the black area. In this case, the output voltages of coefficients coincide with a numerical simulation. If we deal with these outputs as Hadamard coefficients, the image is reconstructed (Fig. 10(d)) by the inverse Hadamard transform (cf. Eq. (6)).

The reconstructed image is quite similar to the input image. Thus we can confirm the basic operation of the Hadamard transform.

In order to evaluate the linearity of the Hadamard transform chip, the measurement method shown in Fig. 11 is devised. The Hadamard base is selected such that the left side is +1 and the right side is -1, as shown in Fig. 11. When an optical power is applied to a +1 pixel, the cell outputs positive value. Likewise, when an optical power is applied to -1 pixel, the cell outputs a negative value. On the whole, the chip output depends on the difference between the number of lighted up +1 pixels and that of lighted up -1 pixels. Thirty-three images made by transparent sheets painted partly opaque using the color black are prepared. The No. 0 image provides maximum light with the -1 side, and it will lead to minimum output. The No. 32 image provides maximum light with the +1 side, and it will lead to maximum output. Other images are prepared so that the numbers of lighted up -1 and +1 cells may change gradually.

Figure 12 shows the output versus each image and the errors causing each to differ from an ideal line.

From these measurements, the maximum linearity error is about 1.5%. This error is caused by the manual

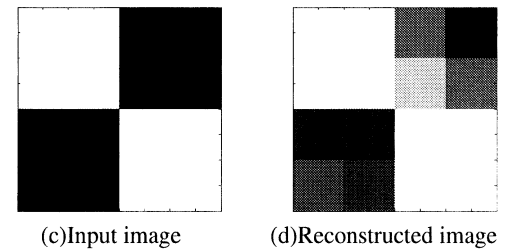
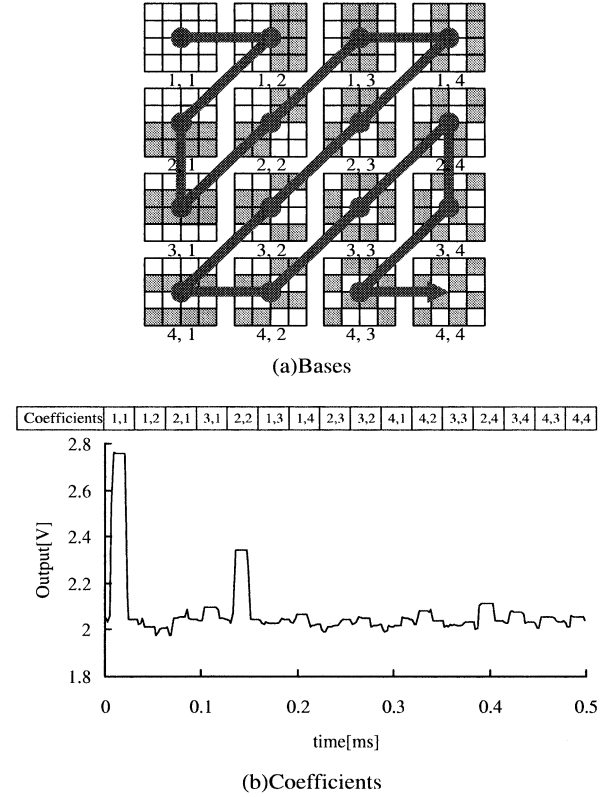


Fig. 10 Coefficients and inverse Hadamard transform result.

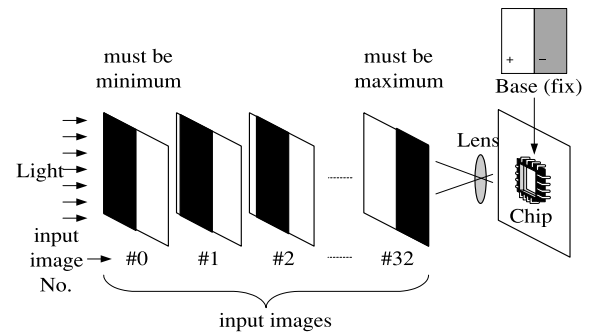


Fig. 11 Linearity measurement method.

alignments of the images and by the lack of uniformity in both input light and edges.

4. Application

We propose a novel technique to calculate the center of

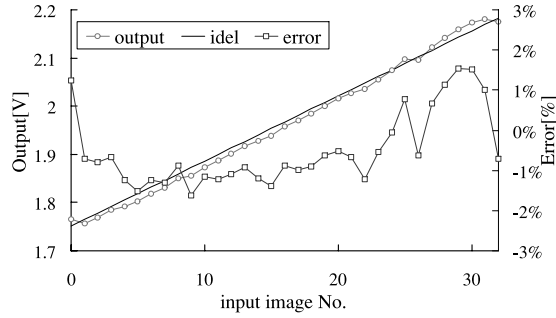


Fig. 12 Linearity evaluation.

gravity using the Hadamard transform chip. For example, we can obtain the y coordinate of the center of gravity g_y , by performing the process shown in Fig. 13(a), using only six coefficients ($64 = 2^6$) as shown in Eq. (7). In addition, the division ($/2, /4, \dots$) is realized easily using a shift resistor. This calculation reduces cost drastically, compared with the cost of conventional calculation. This will become evident as the number of pixels increase. Figure 13(b) shows the results of numerical simulations.

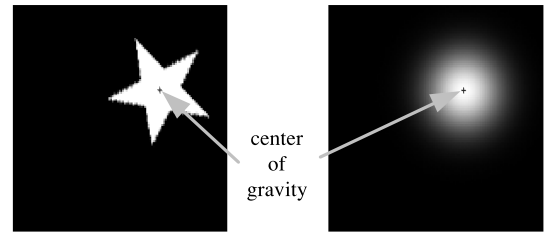
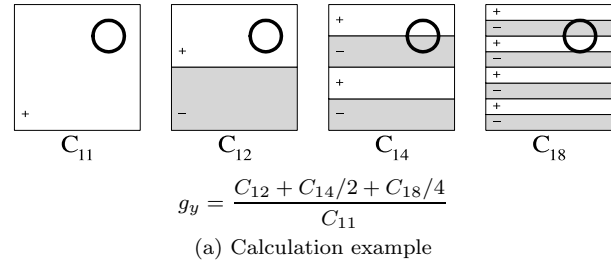
$$g_y = \begin{cases} \frac{\sum_{k=1}^{\log_2 n} c_{12^k} \times 2^{-(k-1)}}{c_{11}} & \text{(Proposed)} \\ \frac{\sum_{j=1}^n j \times \sum_{i=1}^n f(i, j)}{\sum_{i=1}^n \sum_{j=1}^n f(i, j)} & \text{(Conventional)} \end{cases} \quad (7)$$

In this section, we propose the feature of orthogonal transform not restricted to sub-block size. This feature is easily applicable to segmented and normalized images seen in area of pattern recognition.

5. Conclusion

We proposed a novel Hadamard transform circuit using the PWM technique operating on the principle of charge sharing. We confirmed that this circuit achieved high accuracy and high speed when we applied the PWM technique to SPICE simulations. Based on area estimation, we designed and fabricated a test chip containing 64×64 cells to receive pixels. We also designed and fabricated peripheral circuits. We tested the chip through an actual application of image reconstruction, and confirmed that it works. We tested how linear this chip is by gradually changing an image, and thereby estimated that its linearity error is about 1.5%. We demonstrated that the chip drastically reduces the cost of calculating the center of gravity.

We are exploring effective applications of this chip to a machine vision system, and want to investigate



(b) Simulation results

Fig. 13 Center of gravity.

how effective the chip is in actual applications by systematization.

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The VLSI chip in this study was fabricated in the chip fabrication program of the VLSI Design and Education Center (VDEC), the University of Tokyo, with the collaboration by the Rohm Corporation and the Toppan Printing Corporation.

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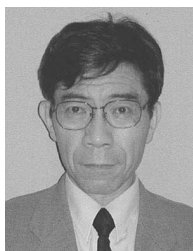
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